

LG3/5 (14"/15.6") MUXLESS and UMA. BLOCK DIAGRAM⁰¹

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

DDR3-SODIMM1
PAGE 12

DDR3 800,1066,1333,1600 MT/s

DDR3-SODIMM2
PAGE 13

DDR3 800,1066,1333,1600 MT/s

Intel Ivy Bridge CPU 45Watt 35Watt
4 Core
(rPGA 989)
PAGE 2-5

VRAM DDR3 *4/*8
(1Gb / 2Gb)
PAGE 19-20

AMD
Thames-Pro/LP 128bit Seymour-XT 64bit
29mm X 29mm
PAGE 14-18

DMI2.0*4

FDI

32.768KHz

PCH 3.5Watt
Platform Controller Hub
PAGE 6-11

SATA HDD 1ST
PAGE 23

SATA0 6.0 Gb/s

SATA - CD-ROM
PAGE 23

SATA2 3.0 Gb/s

LVDS Interface

CRT Interface

HDMI Interface

USB3.0 Interface(12Mbps)

USB2.0 (48Mbps)

(0,9,11)

USB2.0 Port
PAGE 26

USB2.0 Port
USB Charge support
PAGE 26

(1)

BlueTooth
PAGE 28

(8)

Fingerprint
PAGE 28

(12)

Webcam w/ Mic
PAGE 21

(2)

USB3.0 Port x 2
PAGE 26

(10)

half size mini-card
Wireless LAN
PAGE 22

Accelerometer Sensor
LIS3DHTR
PAGE 26

SMBUS

LPC

TPM
SLB9635TT1.2
PAGE 28

32.768KHz

LPC

Keyboard Touch Pad
PAGE 28

ITE KBC
ITE 8518/HX
PAGE 29

SPI ROM EC FW
PAGE 29

System BIOS SPI ROM
PAGE 7

Audio
ALC269Q-VC2-GR
PAGE 24

PCI-E 100M

Azalia

LAN
Atheros AR8161
PAGE 25

25MHz

RJ45
PAGE 25

Card Reader
Realtek RTS5209
PAGE 24

7-in-1 flash media slot(SD/ SDHC / SDXC(UHS 104) / MS/MMC/ XD/MSP)
PAGE 24

Jack to Speaker
PAGE 24

www.schematic-x.blogspot.com

Charger (OZ8682)
PAGE 30

+1.8V (G9661)
PAGE 35

CPU Core1 (NCP6132B)QC
PAGE 36

3/5VS5 (RT8223P)
PAGE 31

VCCSA (SY8037B)
PAGE 33

CPU Core2 (NCP5911)QC
PAGE 37

+VGA POWER
PAGE 39

DDR III (RT8207)
PAGE 32

+1.05V(RT8240BZ)
PAGE 34

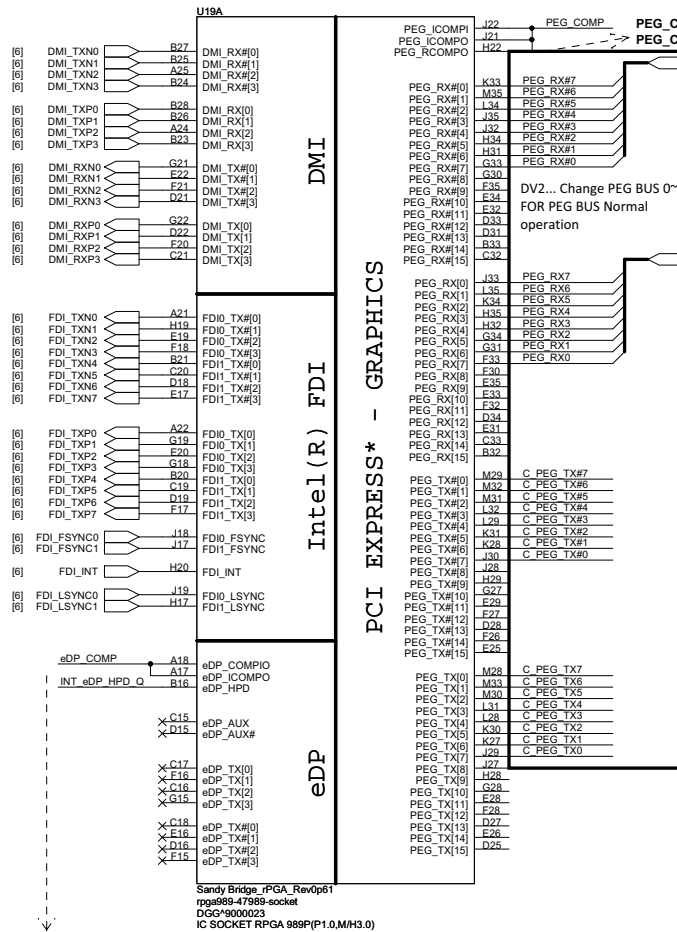
Dis-charge IC (SLG55448VTR)
PAGE 38

+VGACORE (RT8208)
PAGE 40

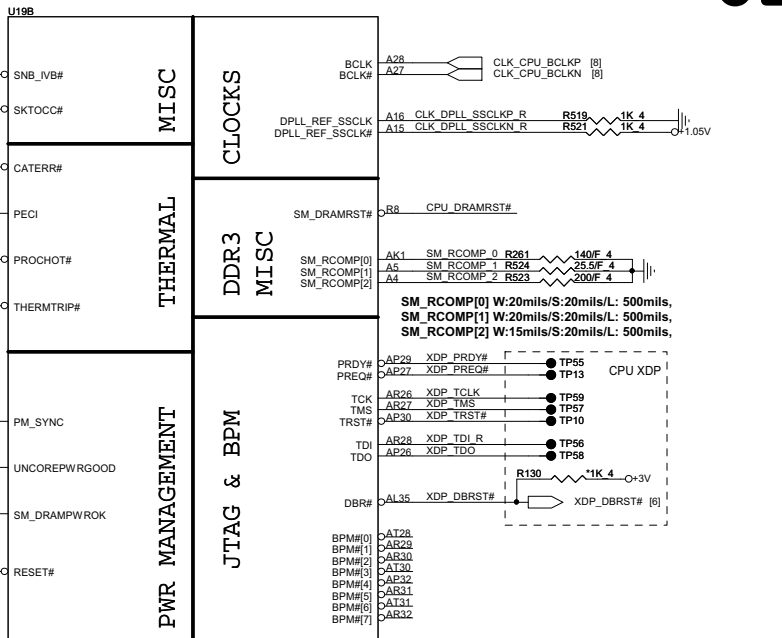
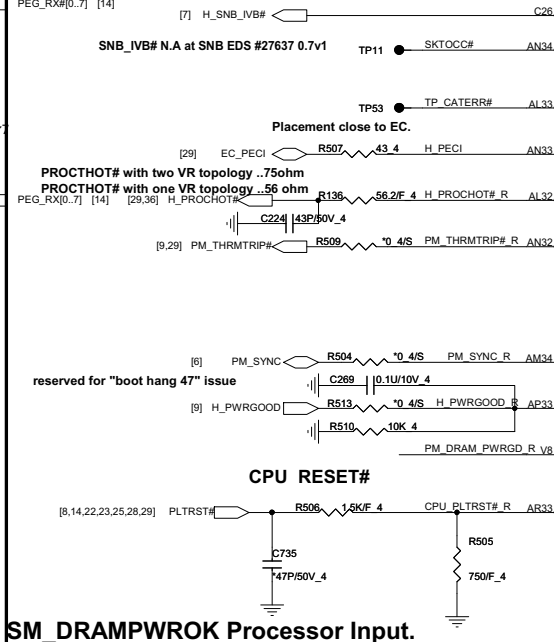


PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

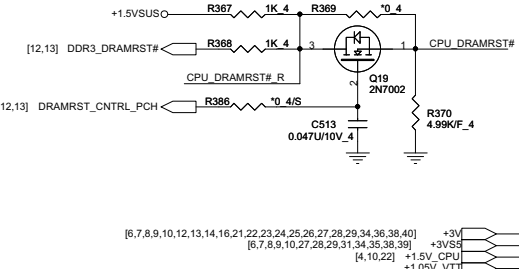
Size Custom Document Number **BLOCK DIAGRAM** Rev 2A
Date: Wednesday, March 07, 2012 Sheet 1 of 42



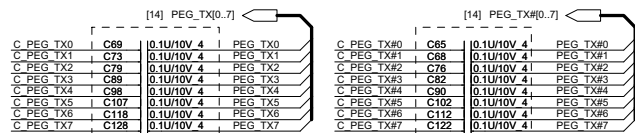
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.



DDR3 DRAM RESET

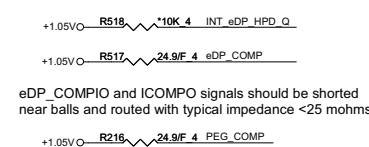


PEG x16 disable (UMA only remove)



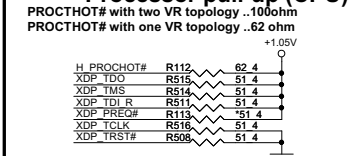
0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation



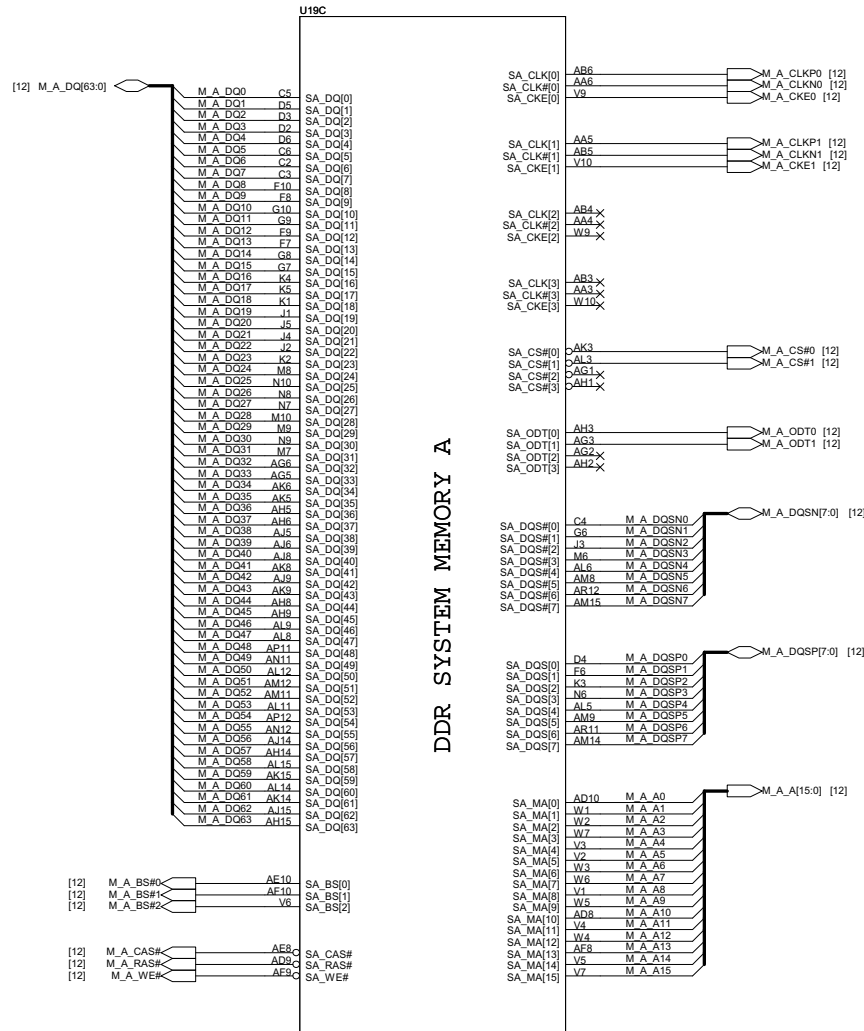
PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

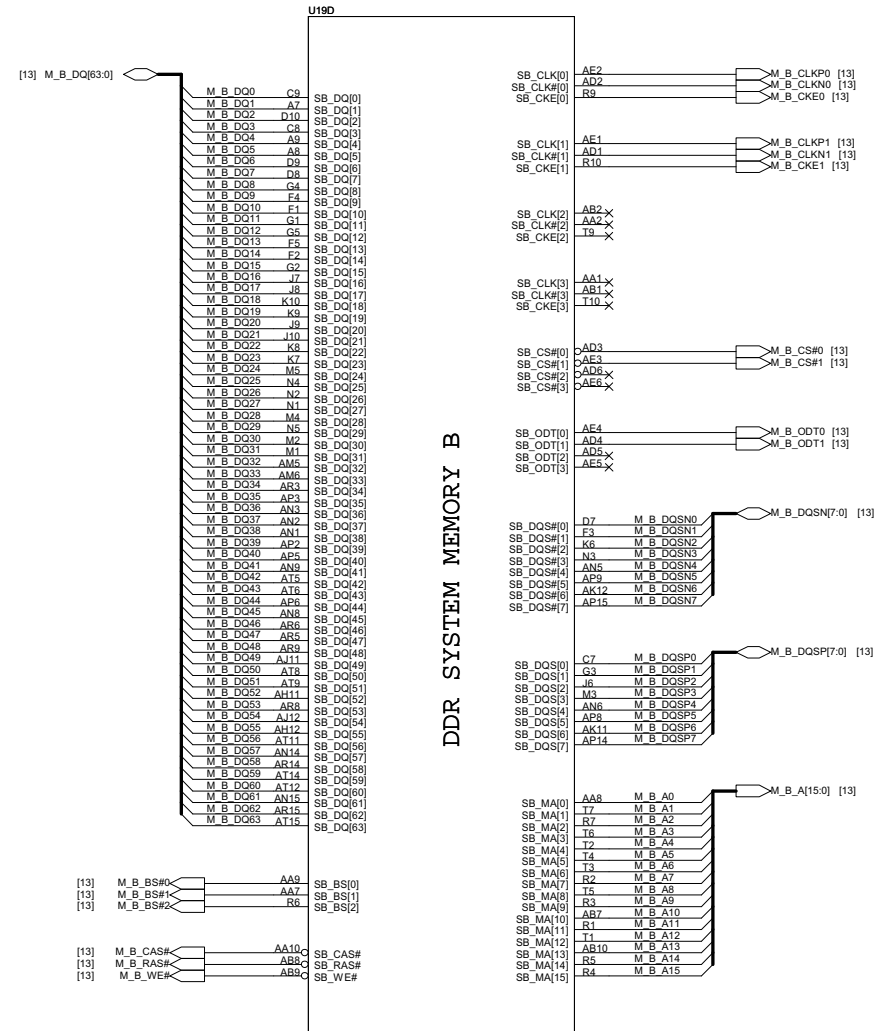


PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)



Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)



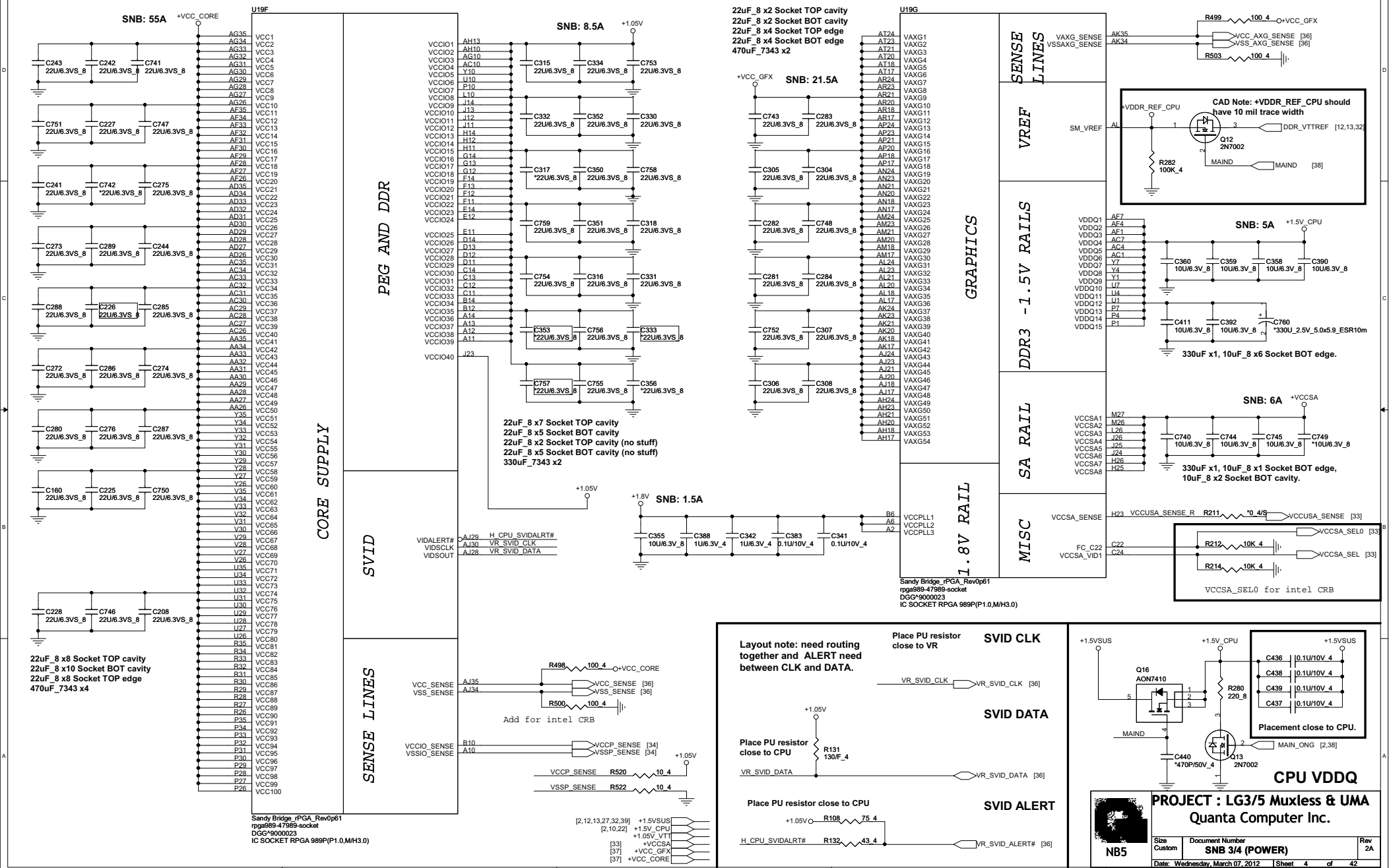
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size Custom	Document Number SNB 2/4 (DDR3 I/F)	Rev 2A
Date: Wednesday, March 07, 2012		Sheet 3 of 42

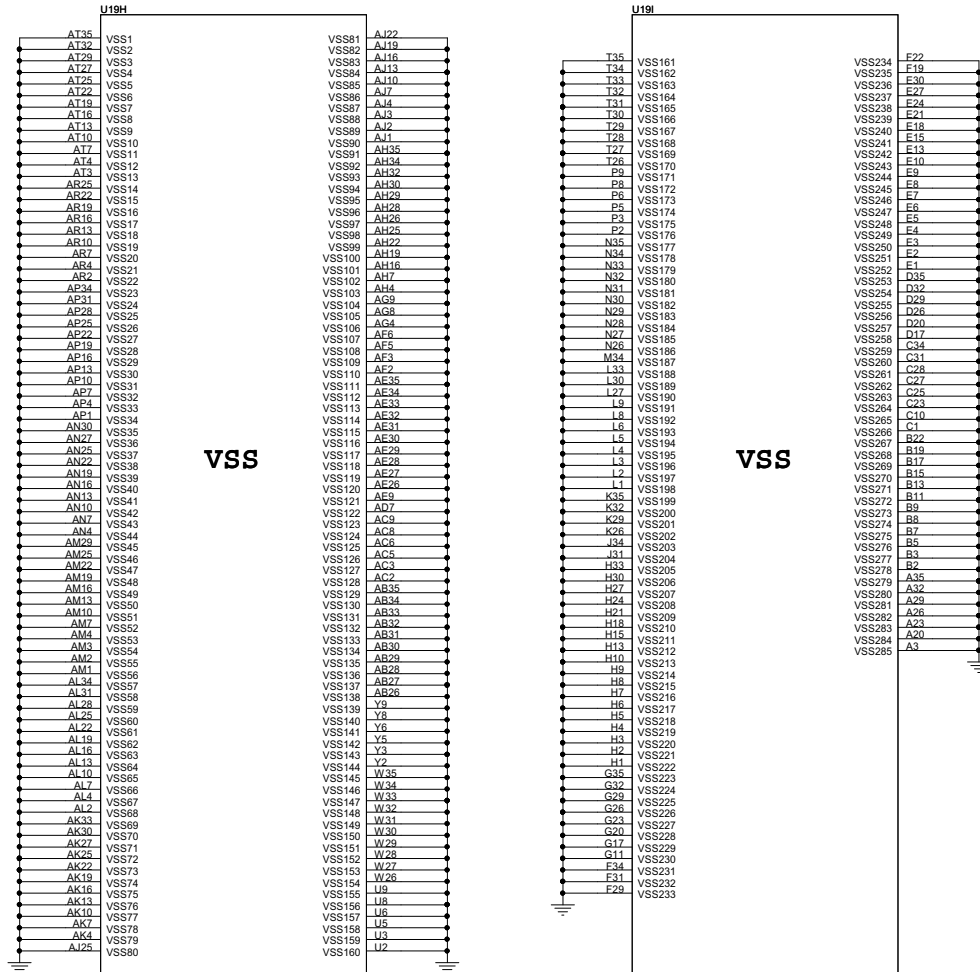
Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04



Sandy Bridge Processor (GND)



Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGP*900023
IC SOCKET RPGA 989P(P1.0,MH3.0)

Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGP*900023
IC SOCKET RPGA 989P(P1.0,MH3.0)

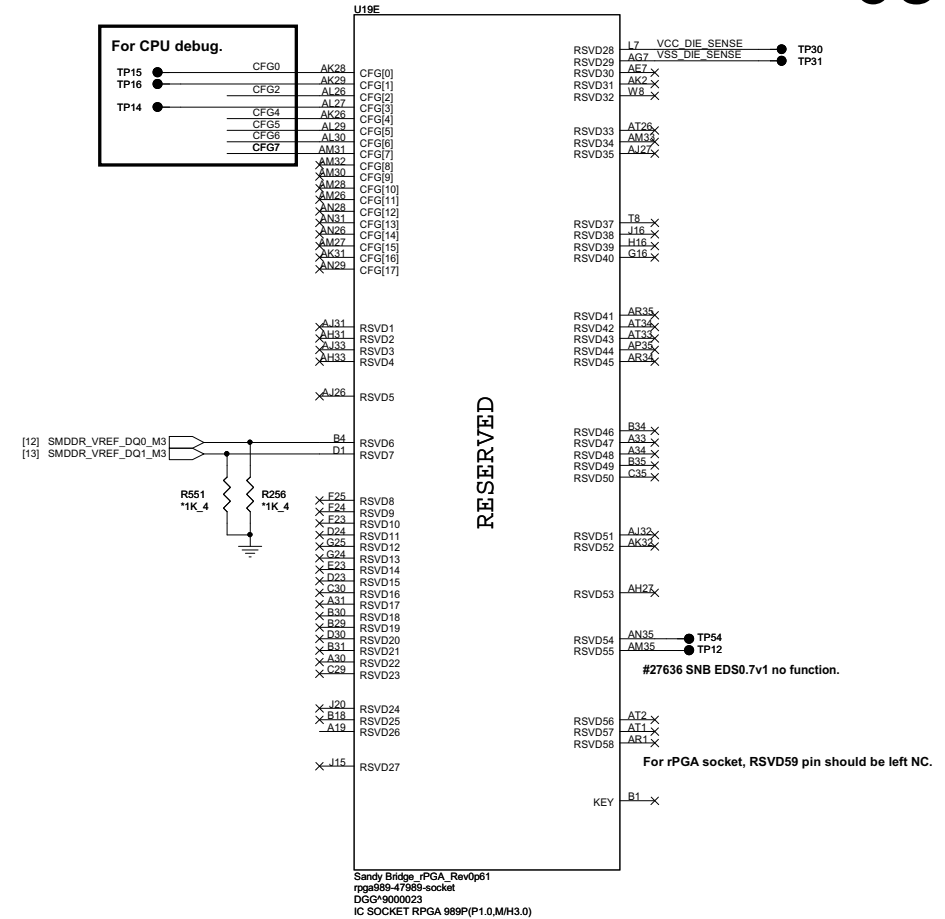
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

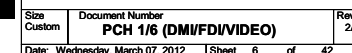
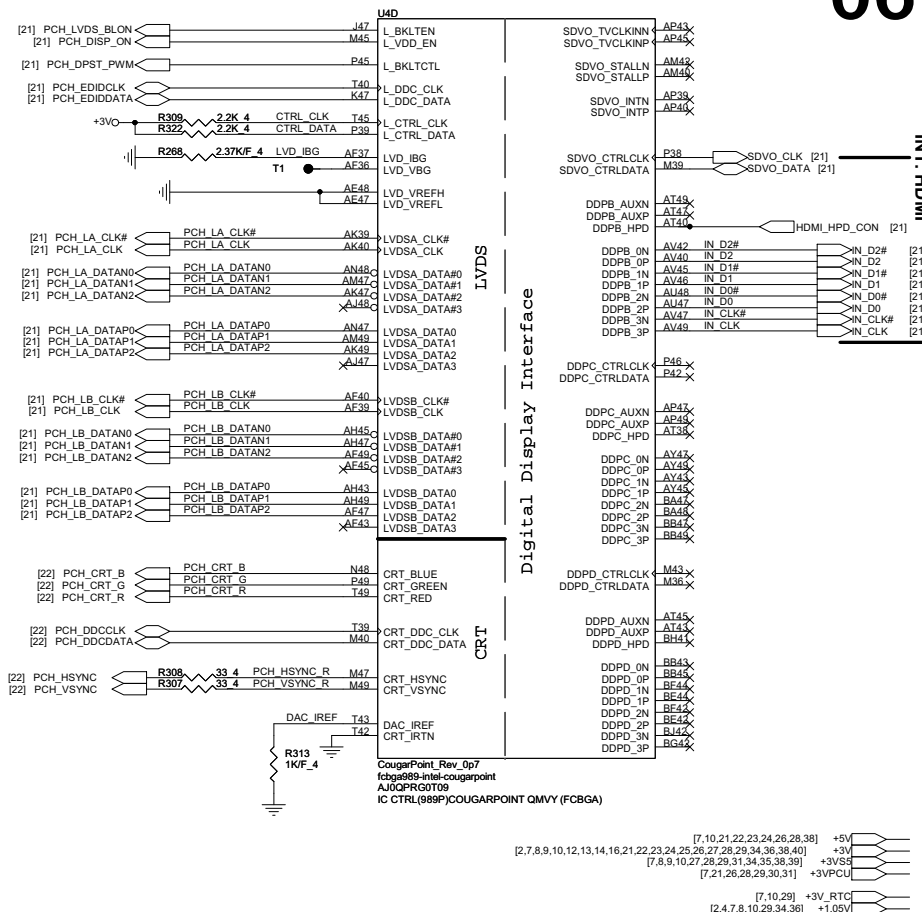
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

Sandy Bridge Processor (RESERVED, CFG)

05

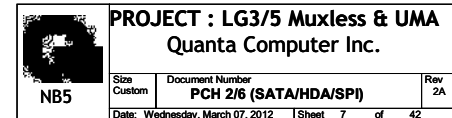


06

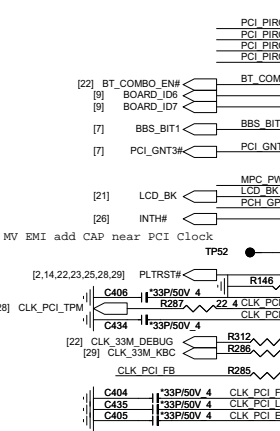
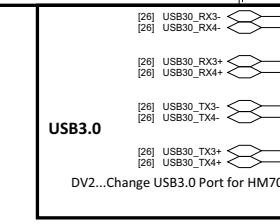
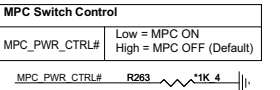
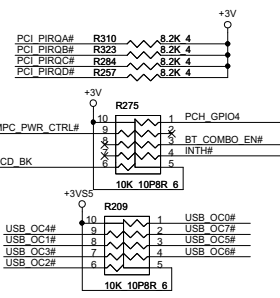


CPU		IO		Peripherals	
CLKGEN_RTC_X1	R221	0.4	RTC_X1	A20	RTCX1
			RTC_X2	D20	RTXC2
			RTC_RST#	C29	RTCRST#
			SRTC_RST#	G22C	SRTCST#
+3V_RTCO	R231	1M	4	SM_INTRUDER#	K22C
			PCH_INVRMEN	C17	INTRUDER#
					INTVRMEN
			ACZ_BCLK	N34	HDA_BCLK
			ACZ_SYNC	L34	HDA_SYNC
[24]	SPKR		SPKR	T10	SPKR
			ACZ_RST#	K34C	HDA_RST#
[24]	ACZ_SDINO			F34	HDA_SDINO
				G34	HDA_SDIN1
				X_C34	HDA_SDIN2
				X_A34	HDA_SDIN3
			ACZ_SDOUT	A38	HDA_SDO
					(+3V)
			GPIO33	C38C	HDA_DOCK_EN# / GPIO33
+3VSSO	R240	1K	4	N32C	HDA_DOCK_RST# / GPIO13
			TP22	J3	JTAG_TCK
			TP47	H7	JTAG_TMS
			TP48	K5	JTAG_TDI
			TP18	H1	JTAG_TDO
[29]	PCH_SPI_CLK		PCH_SPI_CLK	T3	SPI_CLK
[29]	PCH_SPI_CS0#		PCH_SPI_CS0#	Y14C	SPI_CS0#
[29]	PCH_SPI_CS1#		PCH_SPI_CS1#	T1C	SPI_CS1#
[29]	PCH_SPI_SI		PCH_SPI_SI	V4	SPI_MOSI
[29]	PCH_SPI_SO		PCH_SPI_SO	U3	SPI_MISO

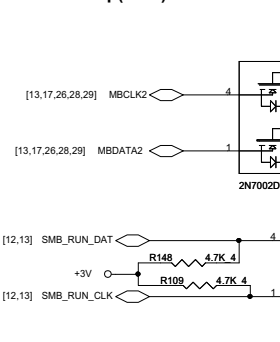
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>SPI</td></tr> <tr> <td>1</td><td>1</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	0	0	SPI	1	1	LPC	<p>[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#</p>
GNT1#	GNT0#	Boot Location											
0	0	SPI											
1	1	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										



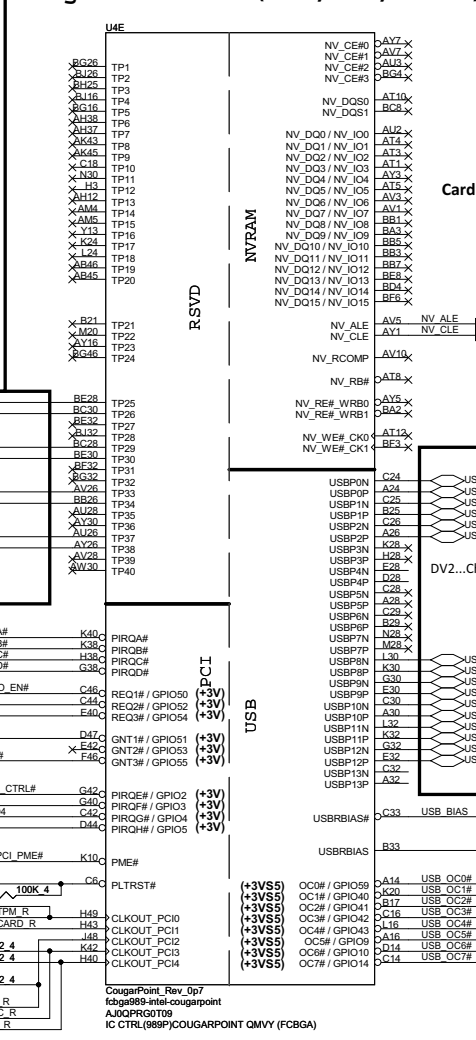
PCI/USBOC# Pull-up(CLG)



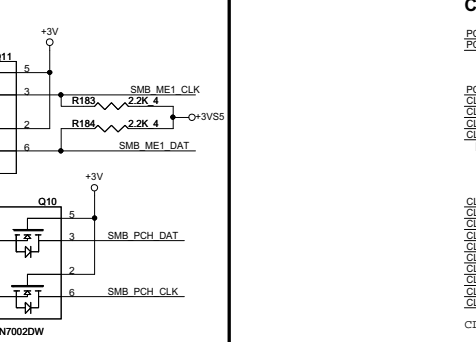
SMBus/Pull-up(CLG)



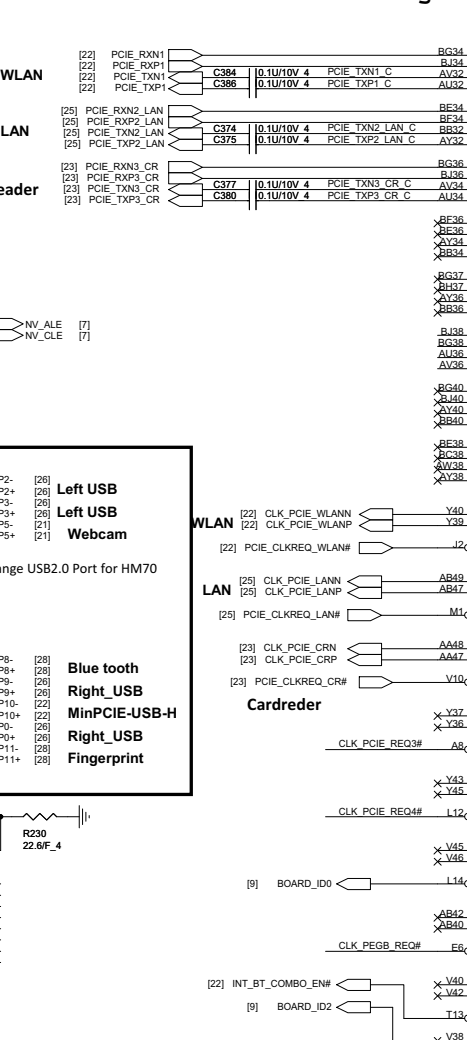
Cougar Point-M (PCI,USB,NVRAM)



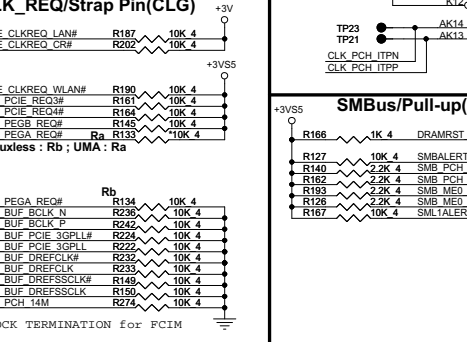
CLK_REQ/Strap Pin(CLG)



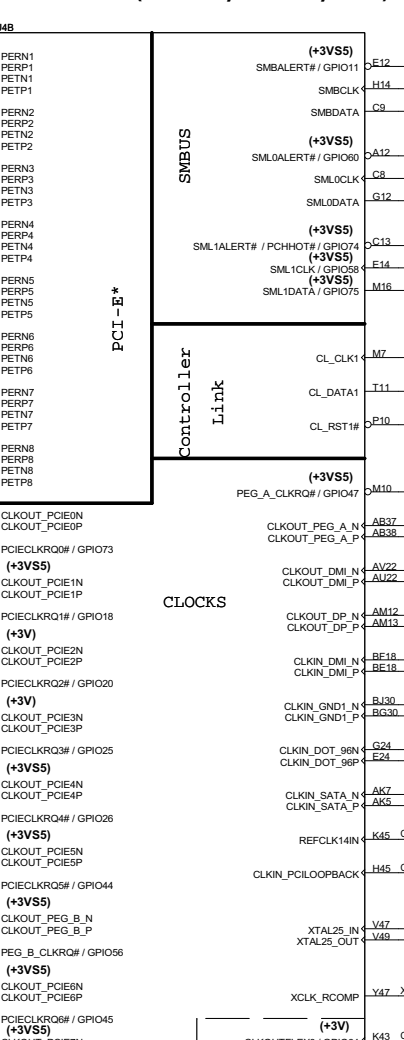
Cougar Point-M (PCI-E,SMBUS,CLK)



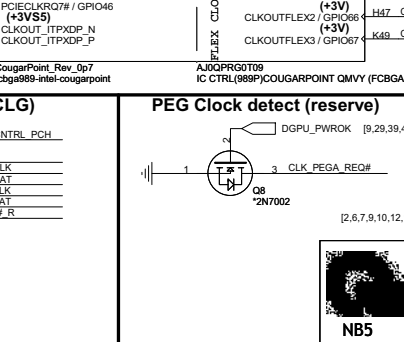
SMBus/Pull-up(CLG)



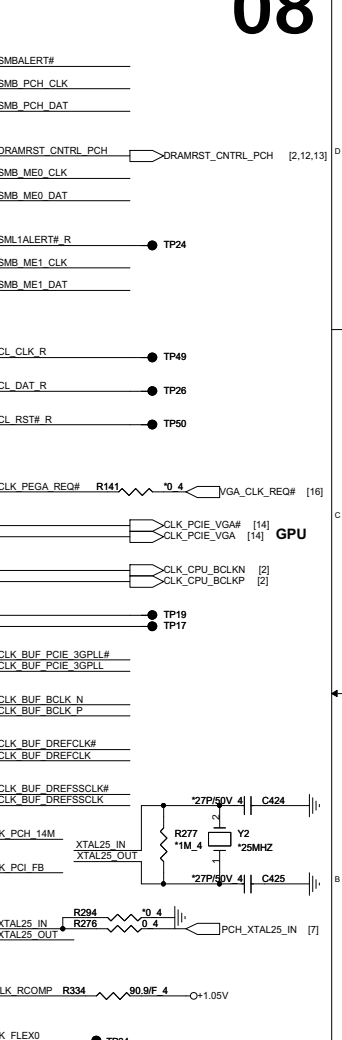
Cougar Point-M (PCI-E,SMBUS,CLK)



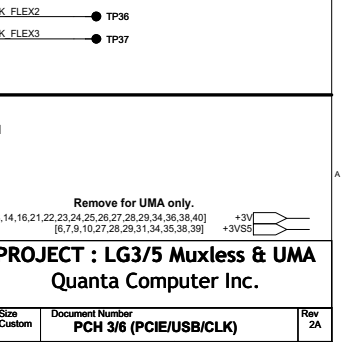
SMBus/Pull-up(CLG)



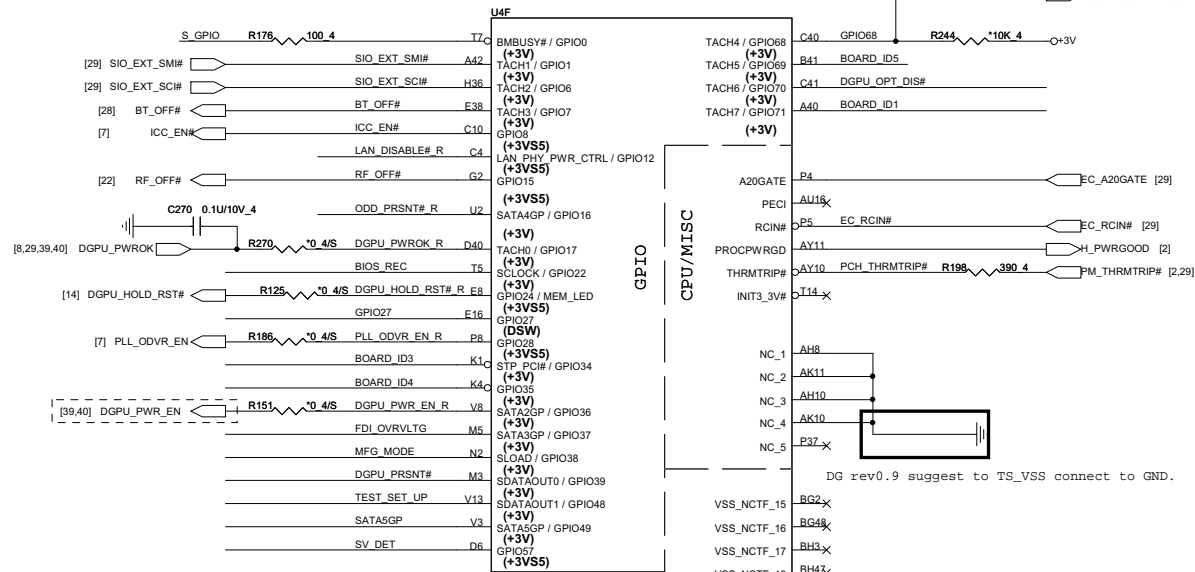
Cougar Point-M (PCI-E,SMBUS,CLK)



SMBus/Pull-up(CLG)



Cougar Point (GPIO,VSS_NCTF,RSVD)

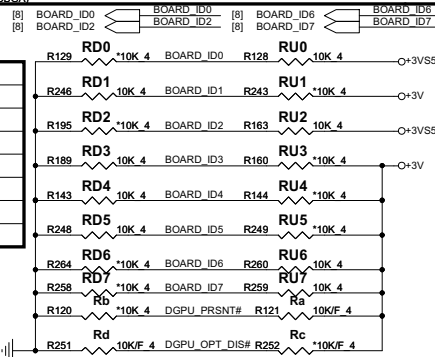


CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AUGPREG0109
IC_CTRL689P/COUGARPOINT.QM.VY.(FCBGA)

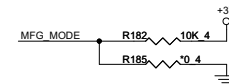
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	Reserve and pull low
BOARD_ID5	GPIO69	Reserve and pull low
DGPU_PRNT#	GPIO39	VGA = 1 , UMA=0
DGPU_OPT_DIS#	GPIO70	Muxless=0, Dis only=1

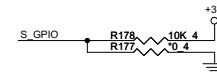
Board ID [3:0]	Model Name
0100	LG3
0101	LG5



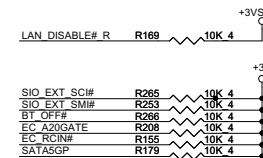
MFG-TEST



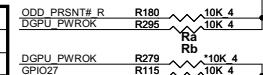
SGPIO



GPIO Pull-up/Pull-down(CLG)



Select	
VGA	Ra
UMA	Rb



Intel ME Crypto Transport Layer
Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

SV_SEF_UP
High = Strong (Default)

TEST DETECT
Low = Default

Only Reserve

DGPU_PWR_EN R R152

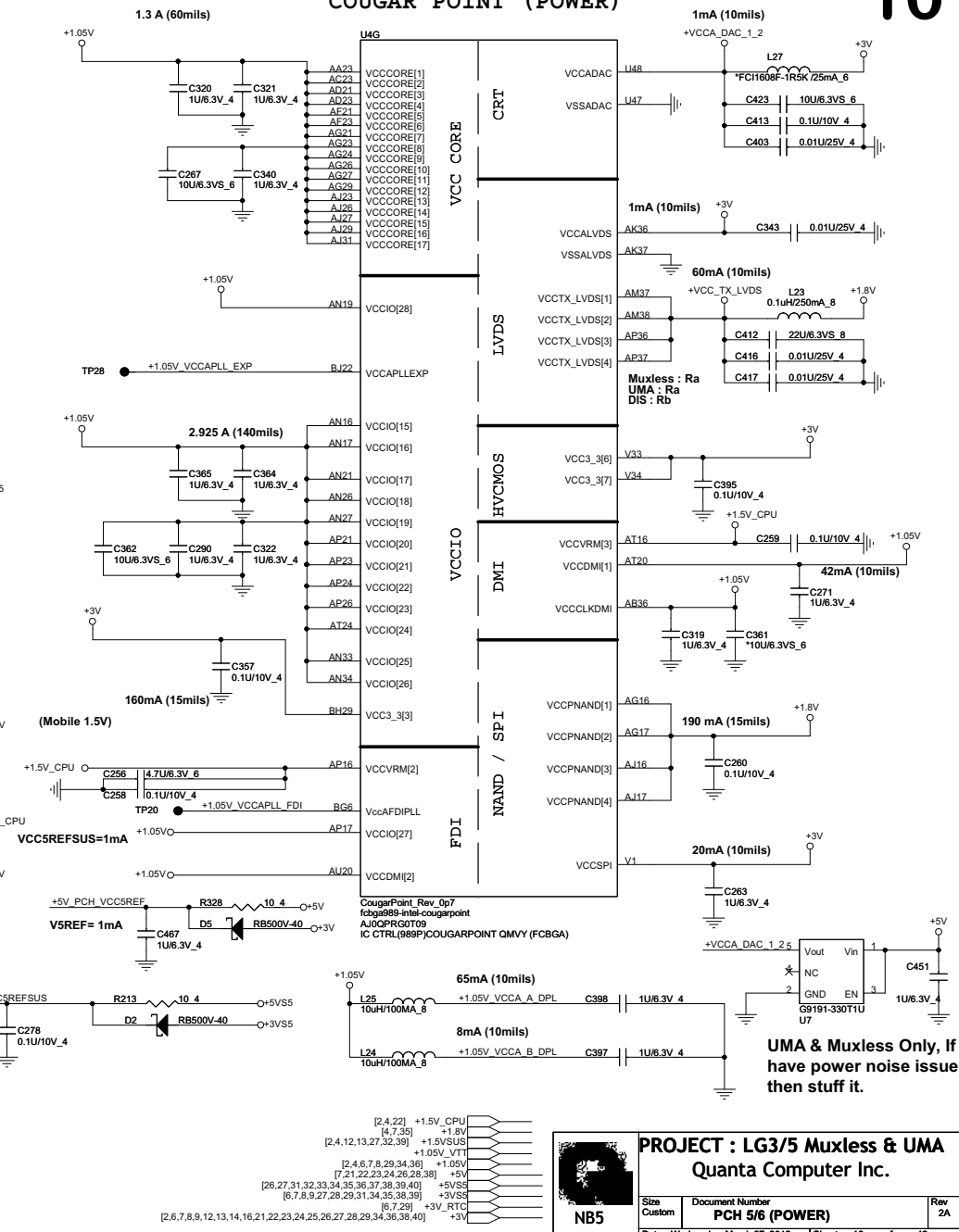
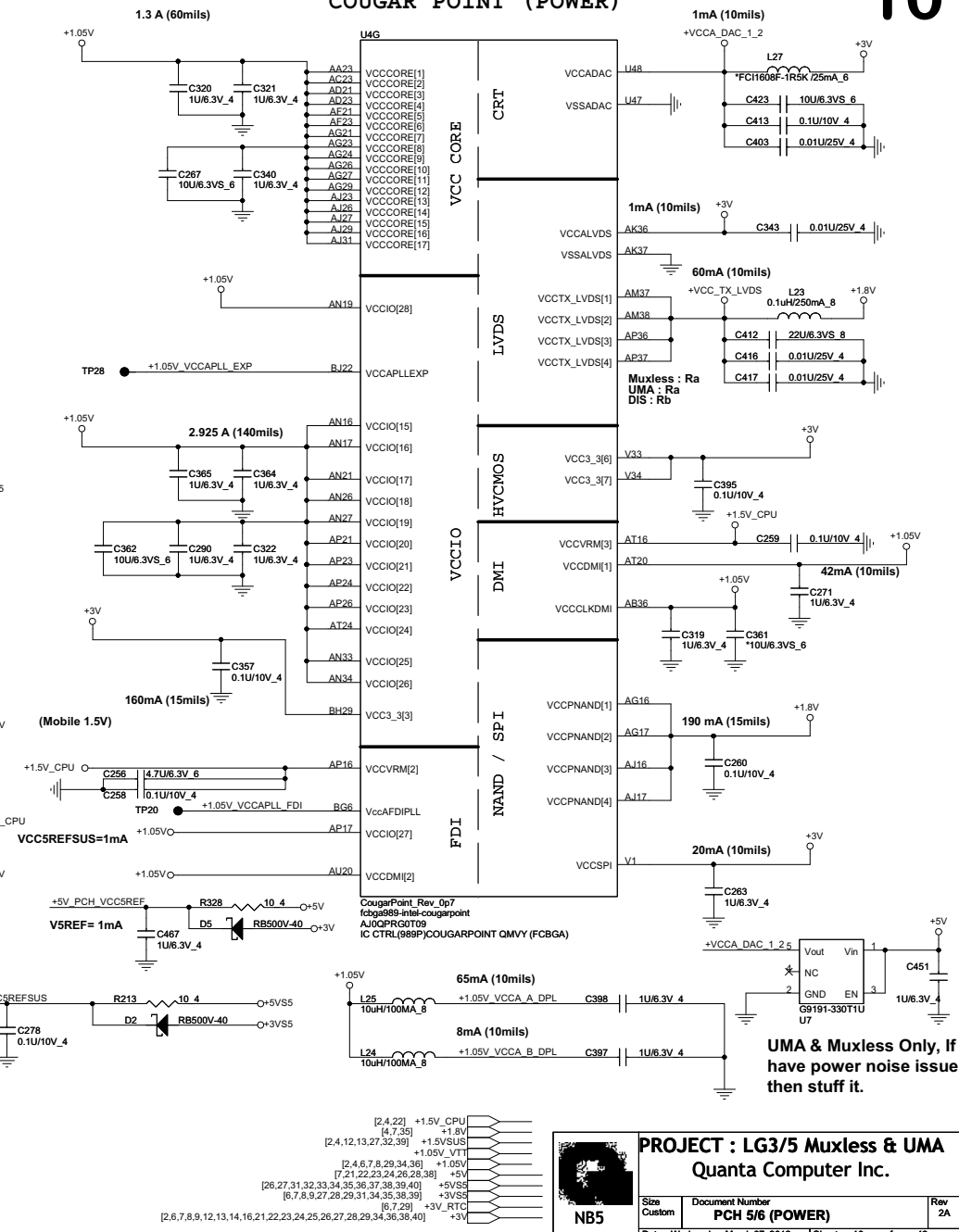
FDI_OVRVLGT R122



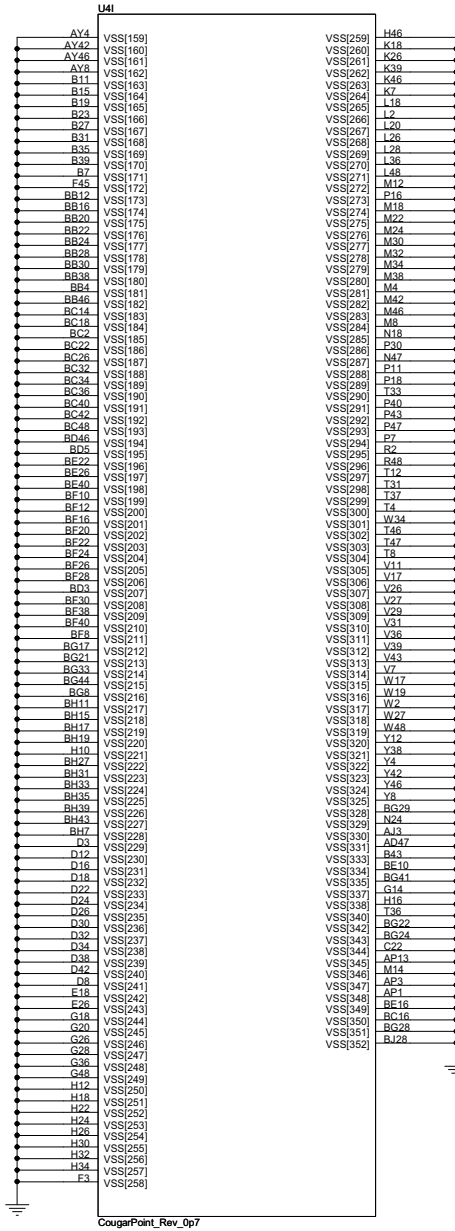
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 2A
Date: Wednesday, March 07 2012 Sheet 9 of 42

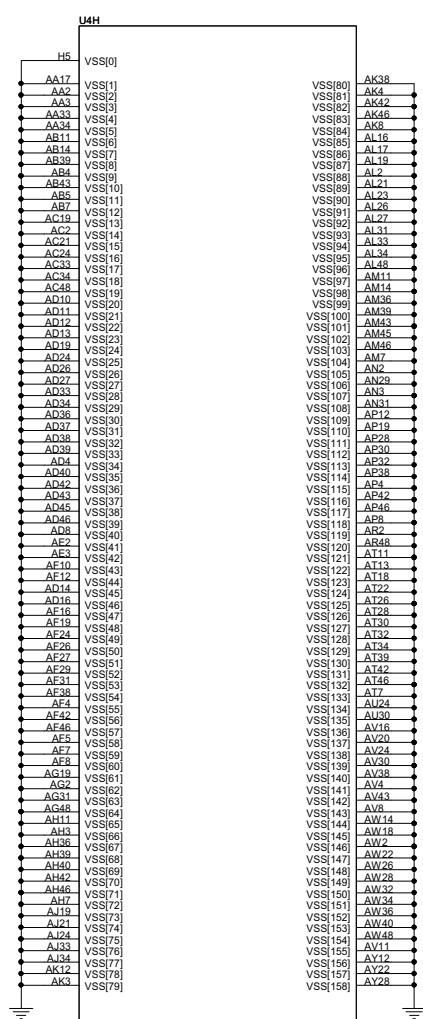
10



IBEX PEAK-M (GND)



IBEX PEAK-M (GND)



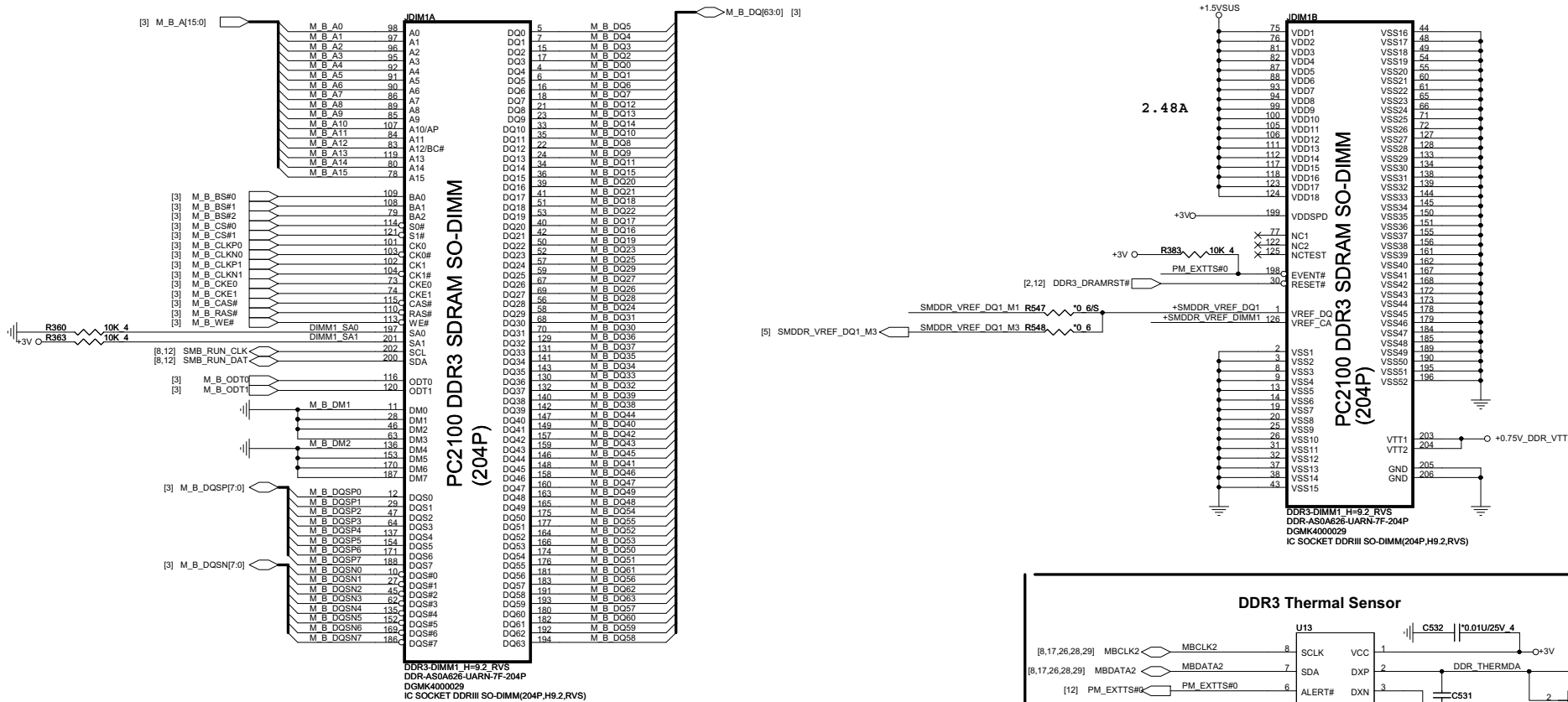


F

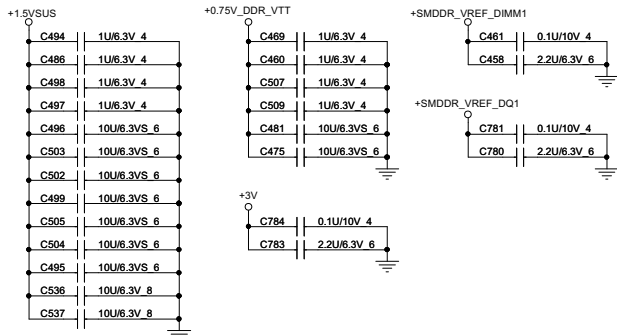


1

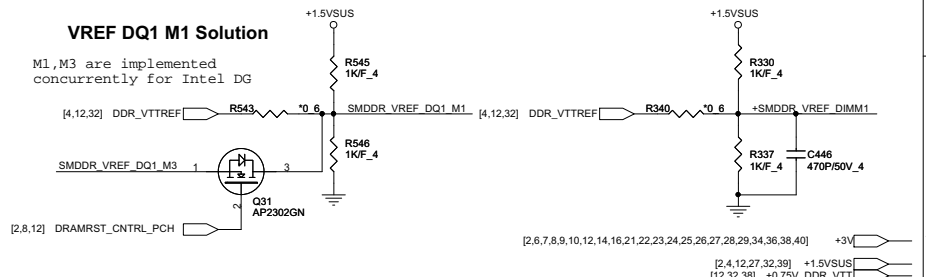




Place these Caps near So-Dimm1.

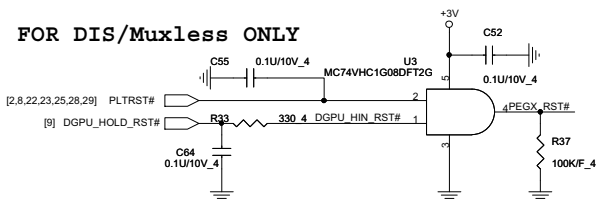


VREF DQ1 M1 Solution



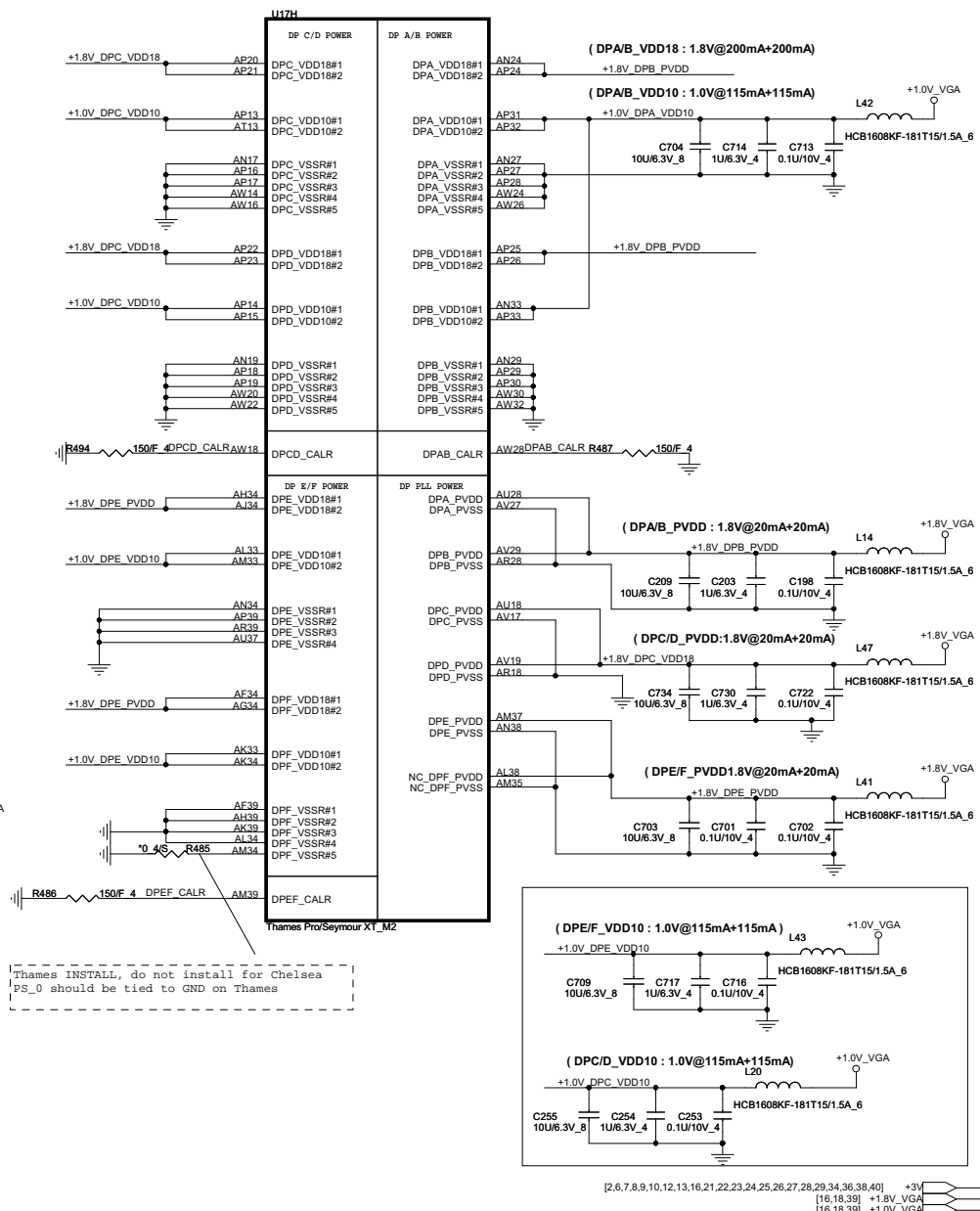
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size Custom Document Number **DDR3 DIMM1-RVS (9.2H)** Rev 2A
Date: Wednesday, March 07 2012 Sheet 13 of 42

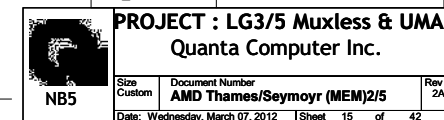


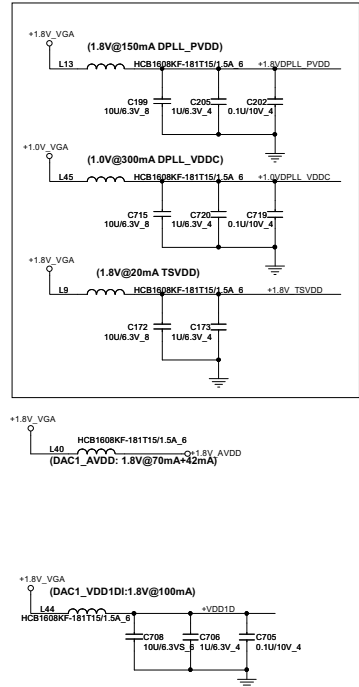
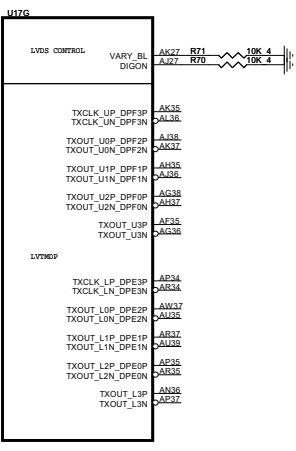
Chelsea		Thames/Seymour
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

```
-----
Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames
```



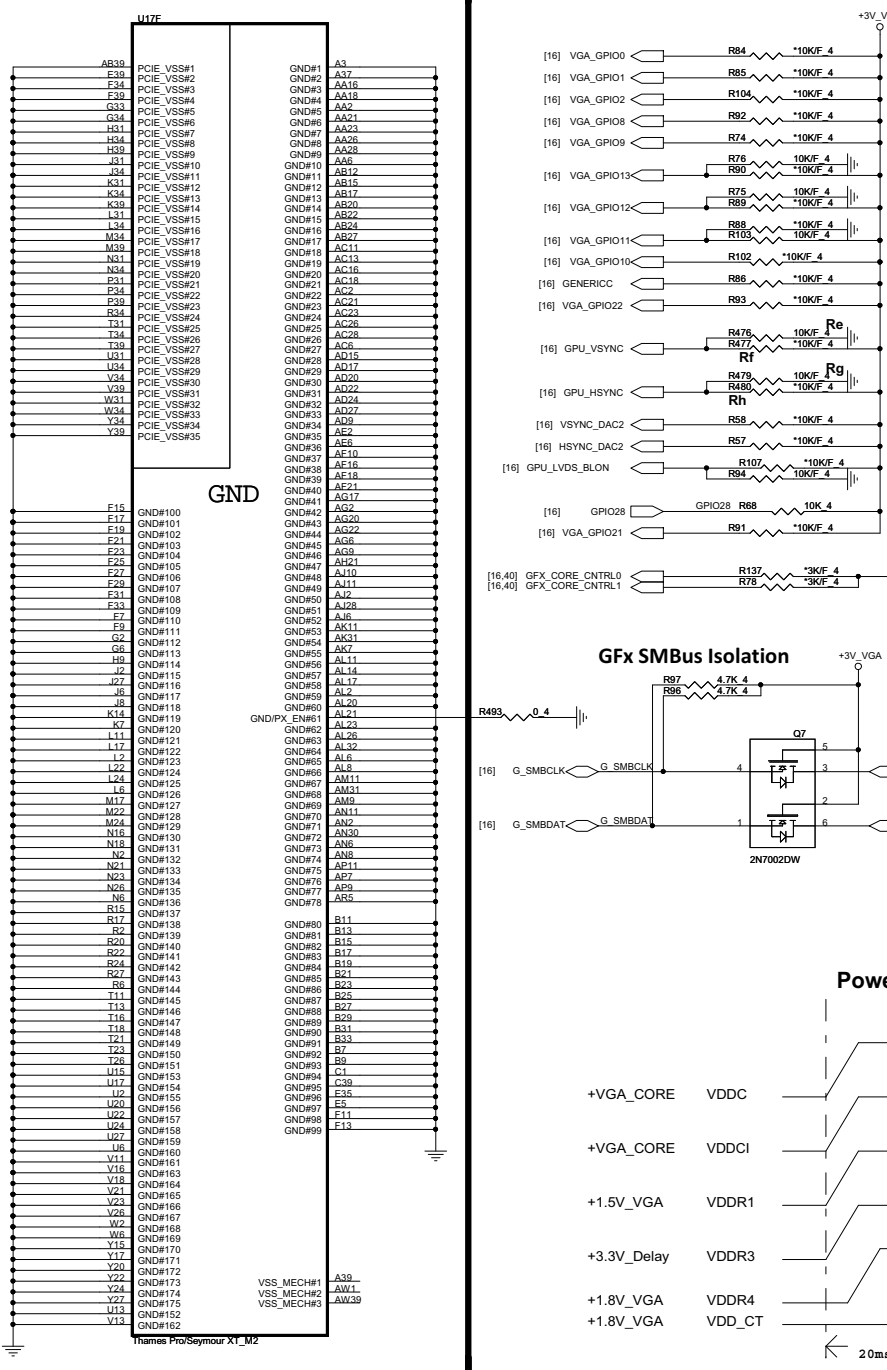
Size Custom	Document Number AMD Thames/Seymour (MEM)1/5	Rev 2A
----------------	---	-----------





Seymour	CNTRL1 GPIO20	CNTRL0 GPIO15
0.9V	0	0
1.05V	1	0
1.15V	1	1

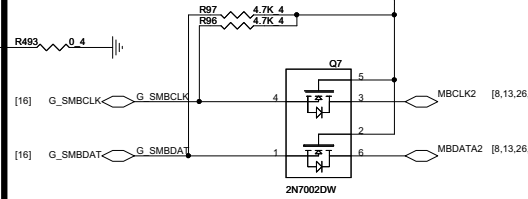
MEM ID	3	2	1	0	DDR3 Type	Configuration	Size
MEM_ID0 Pull High	0	0	0	1	Samsung K4W2G1646C-HC11 (2G bits) Qanta P/N: AKD5MGWT500	128 * 16 x 8 pcs 128 * 16 x 4 pcs	2G 1G
MEM_ID1 Pull High	0	0	1	0	Hynix H5TQ2G63DFR-11C (2G bits) Qanta P/N: AKD5MGWTW16	128 * 16 x 8 pcs 128 * 16 x 4 pcs	2G 1G
MEM_ID2 Pull High	0	1	0	0	Samsng K4W1G1646G-8C11 (1G bits) Qanta P/N: AKD5EGGT500	64 * 16 x 8 pcs 64 * 16 x 4pcs	1G 512M
MEM_ID3 Pull High	1	0	0	0	Hynix H5TQ1G63DFR-11C (1G bits) Qanta P/N: AKDSLZWTW02	64 * 16 x 8 pcs 64 * 16 x 4pcs	1G 512M



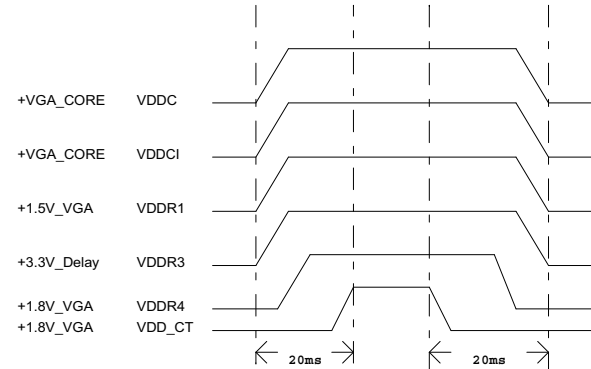
STRAPS

CONFIGURATION STRAPS – SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET																						
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting																		
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X																		
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X																		
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: 1x de-emphasis disabled 1: 1x de-emphasis enabled	X																		
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1																		
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0																		
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type <table><tr><td>100 - 512Kbit</td><td>M25P05A</td><td>(ST)</td></tr><tr><td>101 - 1Mbit</td><td>M25P10A</td><td>(ST)</td></tr><tr><td>102 - 4Mbit</td><td>M25P40</td><td>(ST)</td></tr><tr><td>103 - 16Mbit</td><td>M25P64</td><td>(ST)</td></tr><tr><td>104 - 8Mbit</td><td>M25P80</td><td>(Chingis)</td></tr><tr><td>105 - 128Kbit</td><td>Pm25LV010</td><td>(Chingis)</td></tr></table>	100 - 512Kbit	M25P05A	(ST)	101 - 1Mbit	M25P10A	(ST)	102 - 4Mbit	M25P40	(ST)	103 - 16Mbit	M25P64	(ST)	104 - 8Mbit	M25P80	(Chingis)	105 - 128Kbit	Pm25LV010	(Chingis)	XXX
100 - 512Kbit	M25P05A	(ST)																				
101 - 1Mbit	M25P10A	(ST)																				
102 - 4Mbit	M25P40	(ST)																				
103 - 16Mbit	M25P64	(ST)																				
104 - 8Mbit	M25P80	(Chingis)																				
105 - 128Kbit	Pm25LV010	(Chingis)																				
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X																		
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX																		
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X																		
29,29] RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0																		
29,29] AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX																		

GfX SMBus Isolation



Power Up/Down Sequence



GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

Memory Aperture size

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size Custom Document Number
AMD Thames/Seymour(GD&Str)4/5

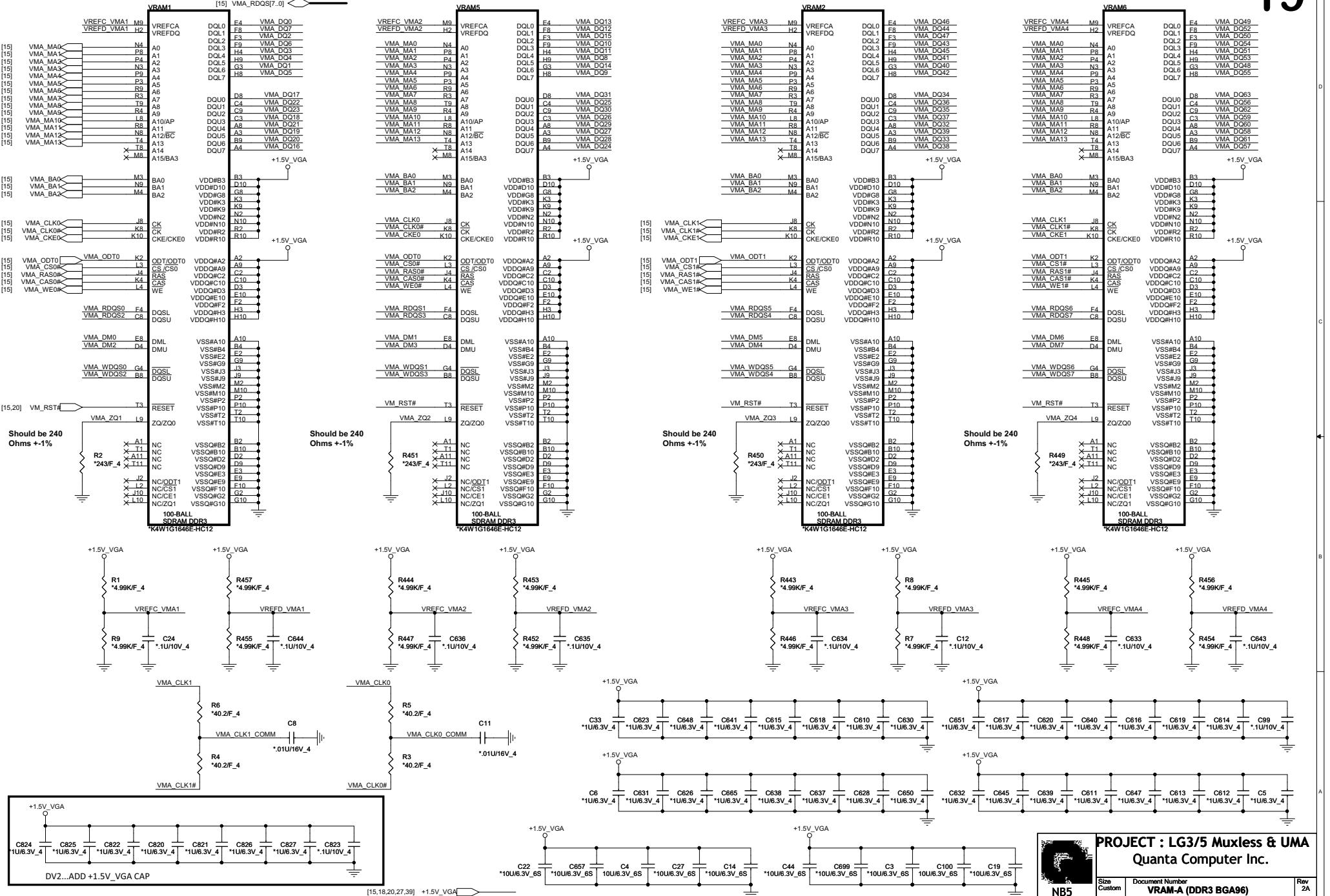
Date: Wednesday, March 07, 2012 1 Sheet 17 of 42



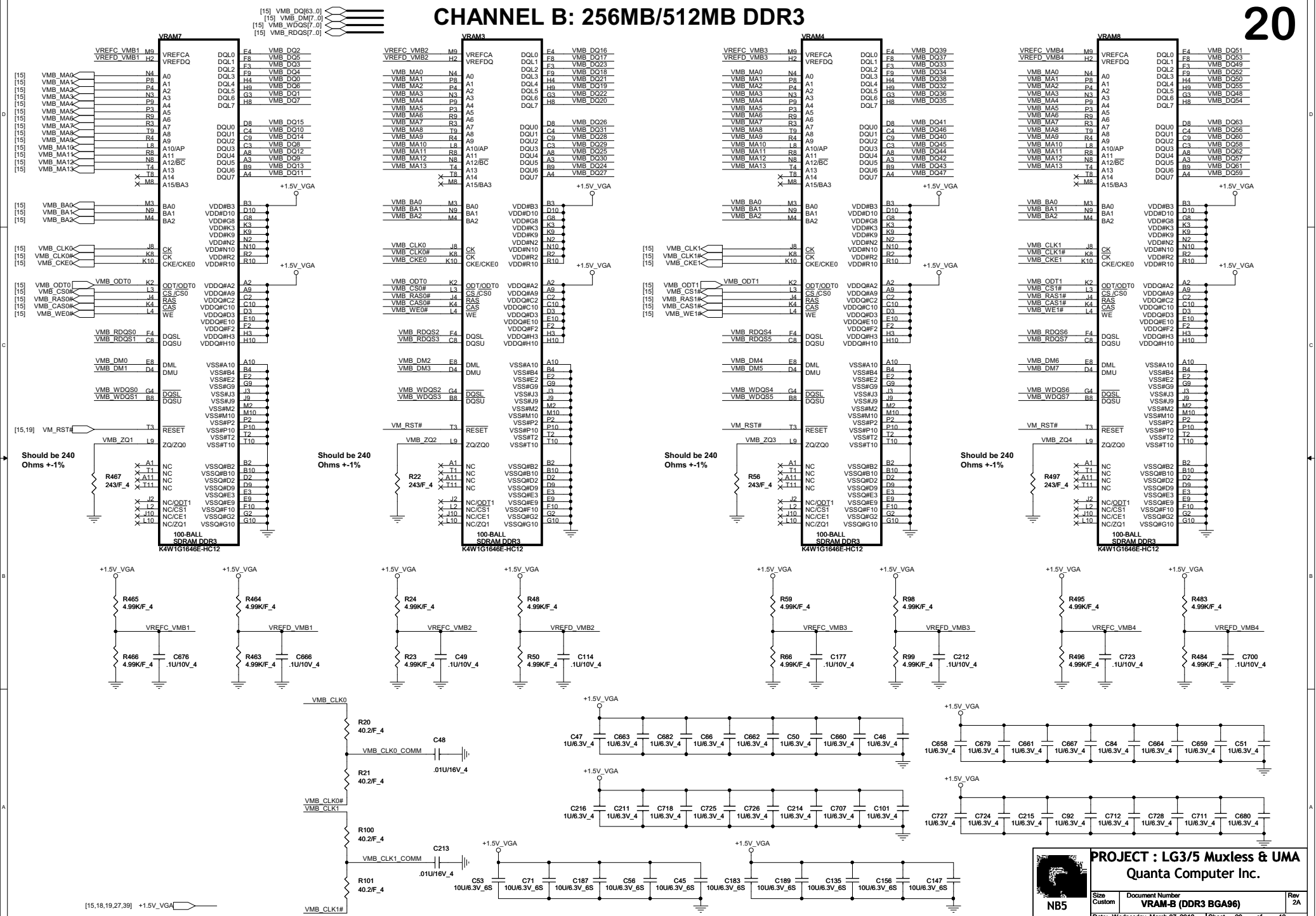
CHANNEL A: 256MB/512MB DDR3

19

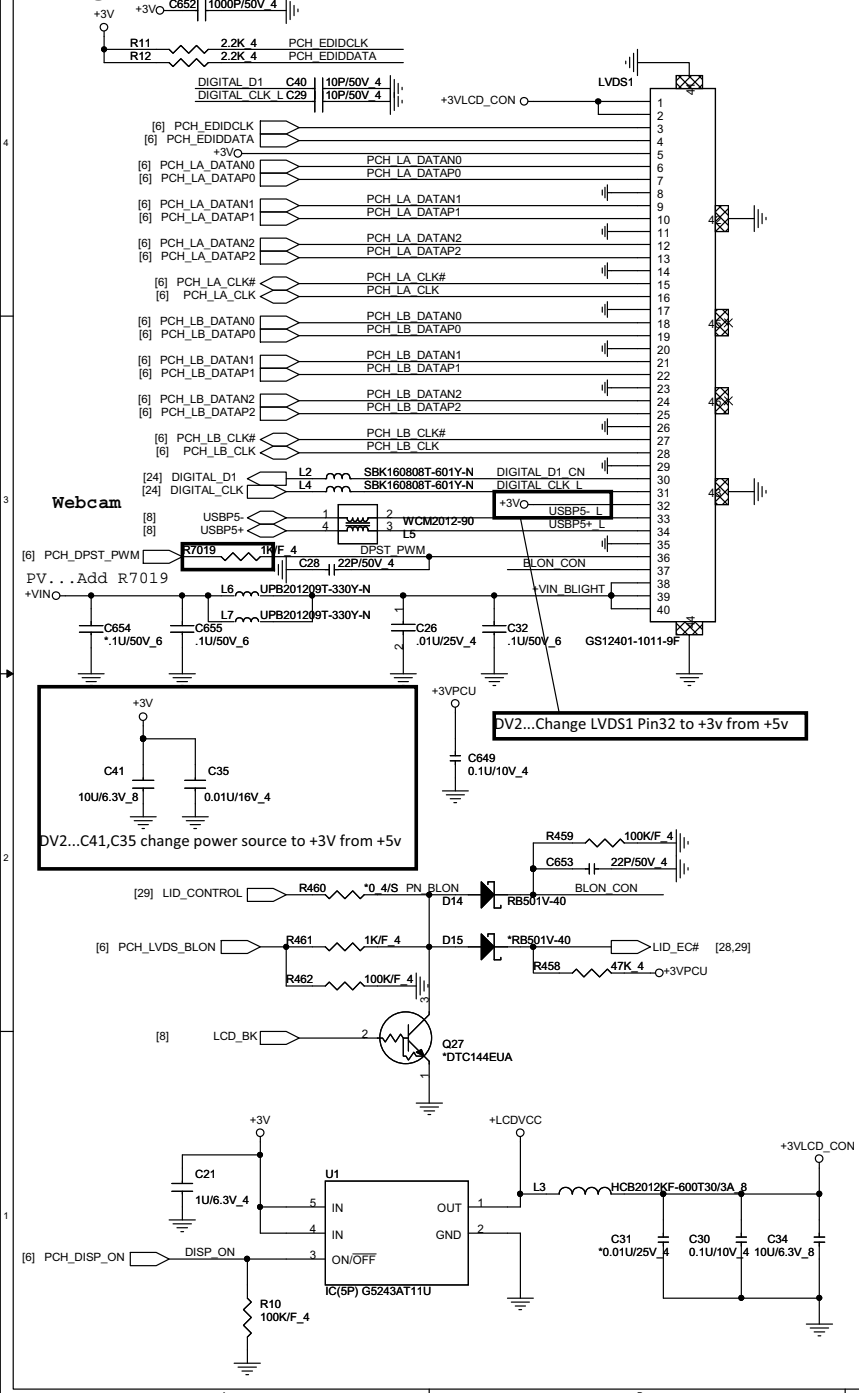
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]



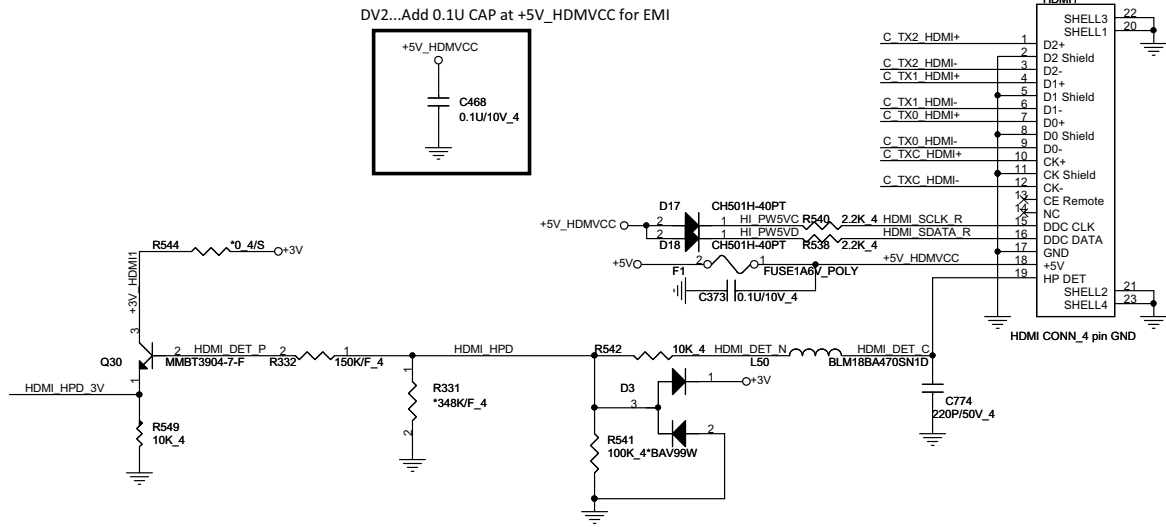
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.



LVDS



HDMI

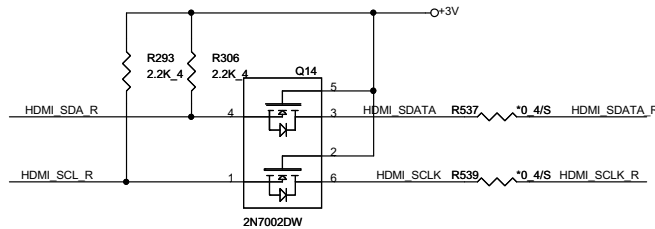


Close connector < 50 mil

EMI

C TXC HDMI+ R245	100/F 4	C TXC HDMI-
C TX0 HDMI+ R255	100/F 4	C TX0 HDMI-
C TX1 HDMI+ R250	100/F 4	C TX1 HDMI-
C TX2 HDMI+ R262	100/F 4	C TX2 HDMI-

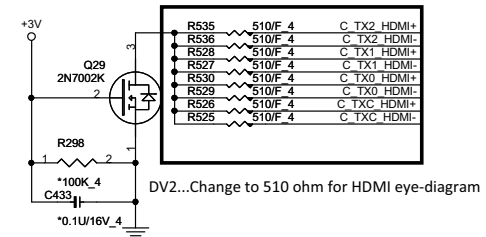
DV2...Change to 100 ohm for HDMI eye-diagram



For Muxless/UMA HDMI function

[6]	IN_CLK#	C376	0.1u/10V 4	C TXC HDMI-
	IN_CLK	C378	0.1u/10V 4	C TXC HDMI+
[6]	IN_D0#	C385	0.1u/10V 4	C TX0 HDMI-
[6]	IN_D0	C387	0.1u/10V 4	C TX0 HDMI+
	IN_D1#	C381	0.1u/10V 4	C TX1 HDMI-
[6]	IN_D1	C382	0.1u/10V 4	C TX1 HDMI+
	IN_D2#	C391	0.1u/10V 4	C TX2 HDMI-
[6]	IN_D2	C389	0.1u/10V 4	C TX2 HDMI+
[6]	SDVO_DATA	R305	*0 4/S	HDMI SDA R
	SDVO_CLK	R292	*0 4/S	HDMI SCL R
[6]	HDMI_HPD_CON	R550	*0 4/S	HDMI HPD 3V

Close connector < 50 mil



PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

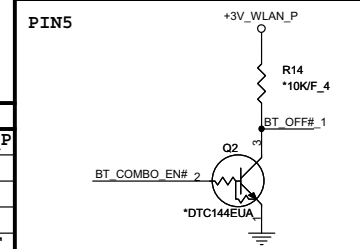
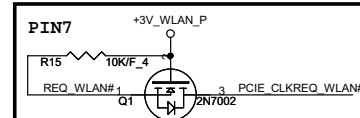
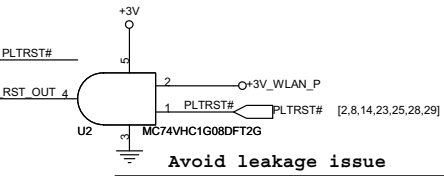
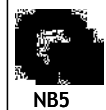
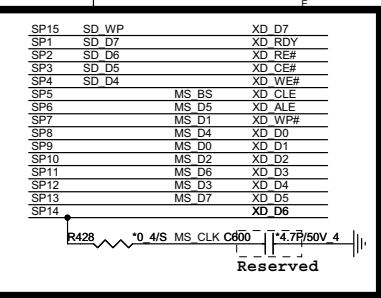


Diagram illustrating the connection of the WLAN LED pin (PIN44) to the 3V_WLAN_P supply and the RF_LINK#3 pin. The circuit includes a 3V_WLAN_P supply, a 2N7002 MOSFET, and the WLAN_LED#1 pin. The MOSFET is connected to the 3V_WLAN_P supply and the RF_LINK#3 pin, with the RF_LINK#3 pin also connected to a 2N7002 MOSFET.

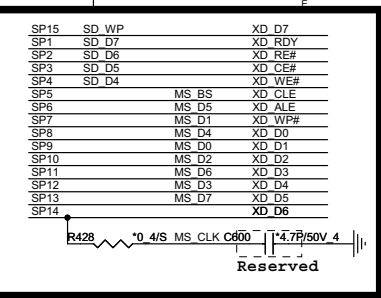
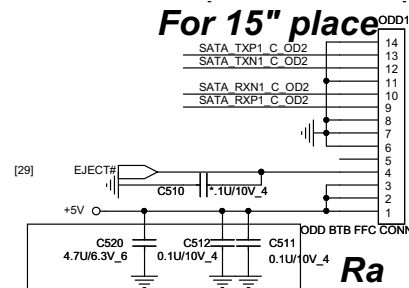
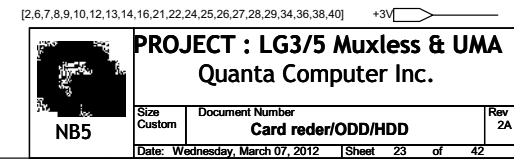
WLAN	Bluetooth	3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF



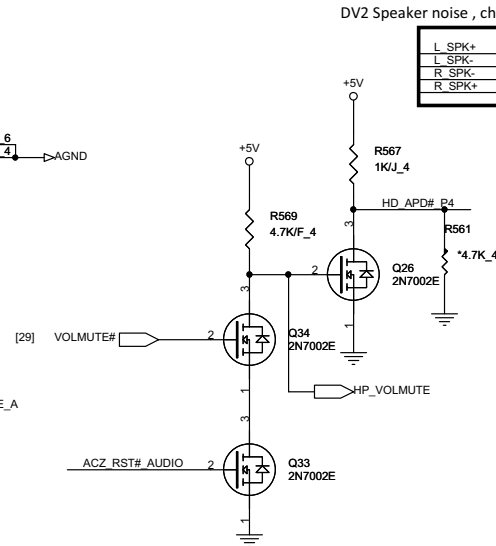
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.



7-in-1
flash media
slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)

***Rb***

4 Ra

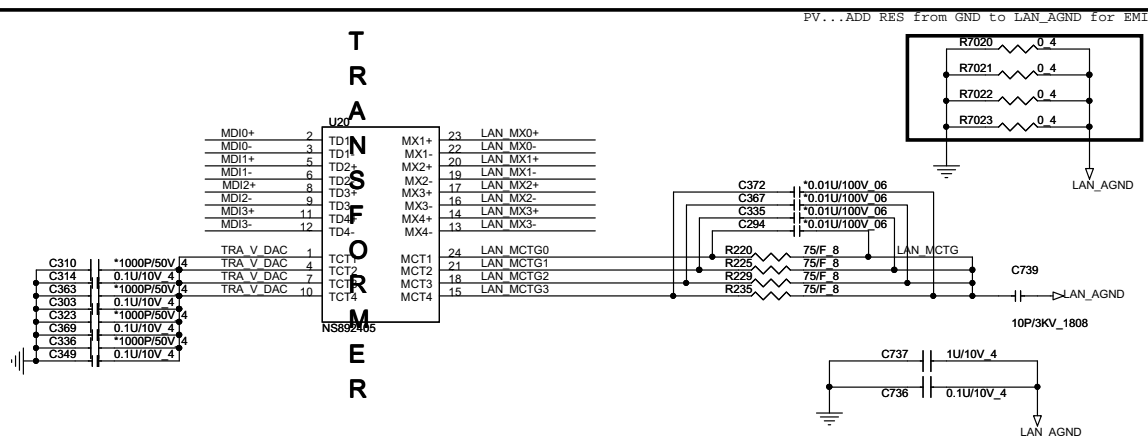
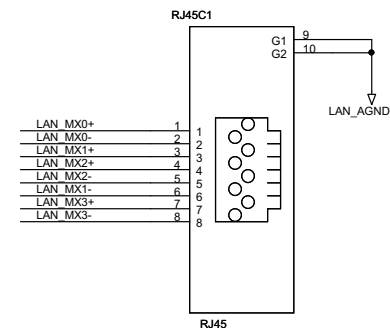
[illegible][illegible]

The schematic diagram illustrates the microphone input section. It features four clamping diodes, labeled CD1, CD2, CD3, and CD4, each connected to a common AGND (Analog Ground) point. The inputs are SENSE MIC, SENSE PHONE, HPOUT_L2, and HPOUT_R2. The outputs are MIC IN R and MIC IN L. The connections are as follows: SENSE MIC is connected to CD6, which is a clamping diode connected to AGND. SENSE PHONE is connected to CD5, which is a clamping diode connected to AGND. HPOUT_L2 is connected to CD2, which is a clamping diode connected to AGND. HPOUT_R2 is connected to CD1, which is a clamping diode connected to AGND. MIC IN R is connected to CD3, which is a clamping diode connected to AGND. MIC IN L is connected to CD4, which is a clamping diode connected to AGND.

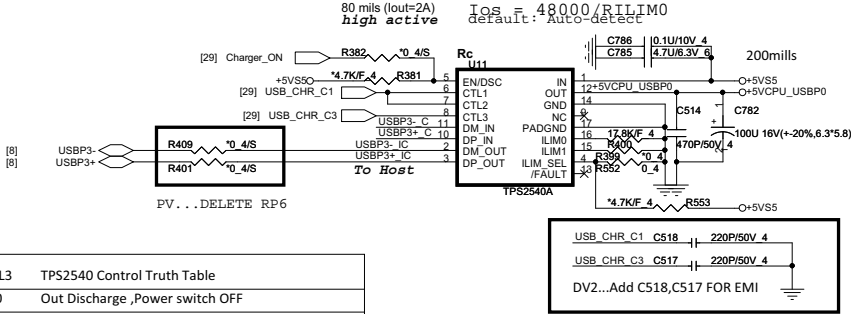


PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size Custom	Document Number HDA Azalia ALC269/Audio Jack	Rev 2A
Date: Wednesday, March 07, 2012		Sheet 24 of 42



Charger USB

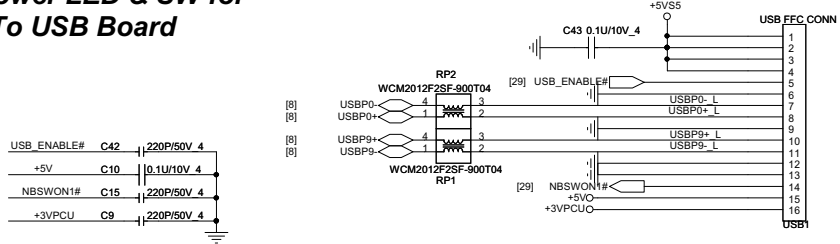


CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge, Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

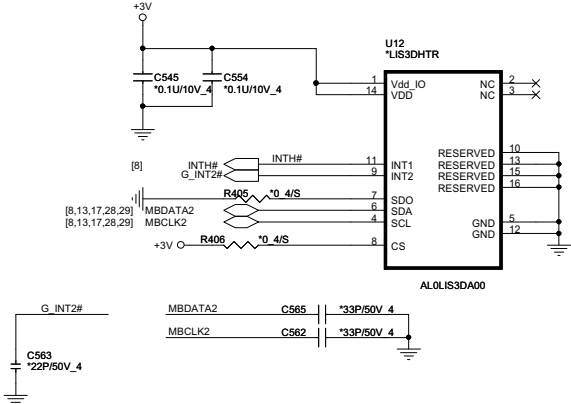
Detect device to Charge:AUTO Detect		
Fast Charge	S0	S3
Enable	CDP	DCP
Disabled	SDP	SDP

Current Battery Capacity	Always-on Charge	S4/S5	
		AC Mode	DC Mode
>Low battery level	Enable	DCP	DCP
	Disabled	OFF	OFF
<=Low battery level	Enable	DCP	OFF
	Disabled	OFF	OFF

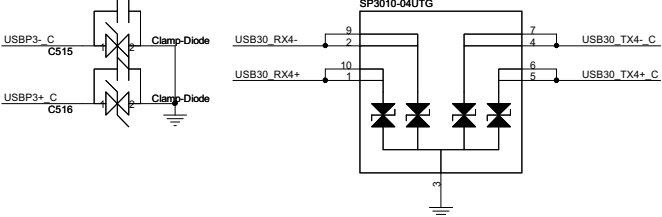
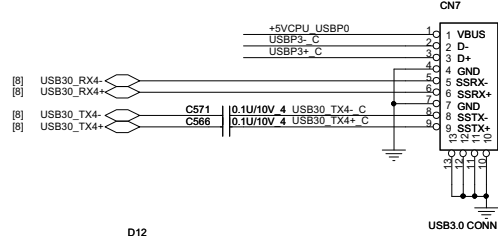
USB / Power LED & SW for 14"/15" To USB Board



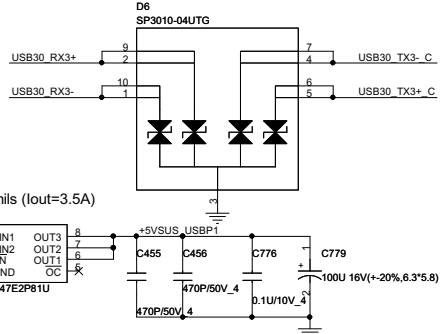
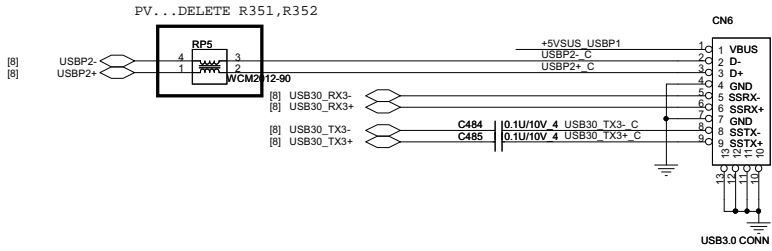
Accelerometer Sensor




USB3.0/USB2.0 x1 COMBO/Charger Port



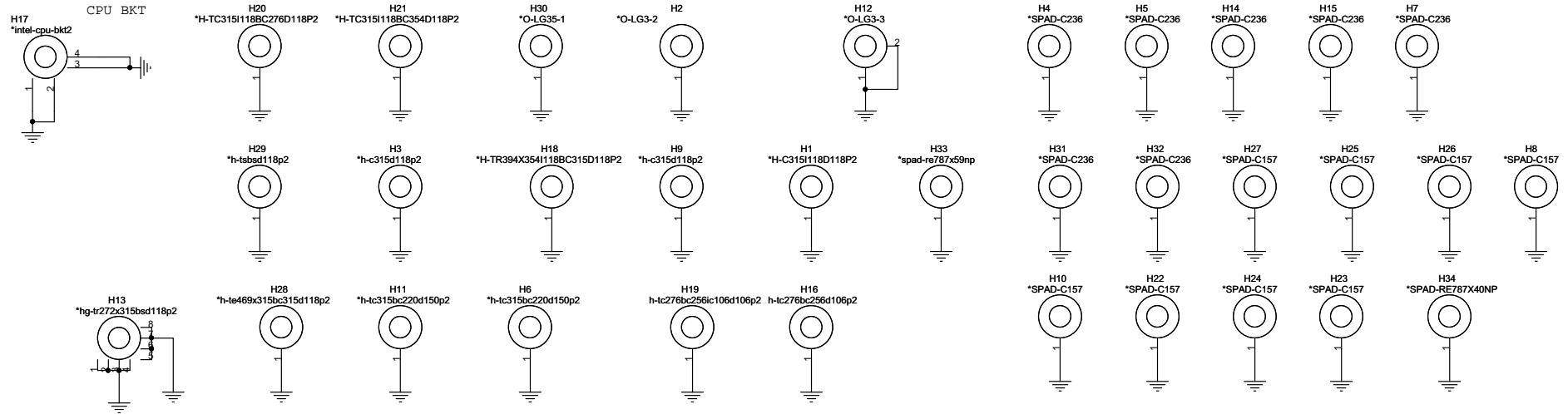
USB3.0/USB2.0 x1 COMBO





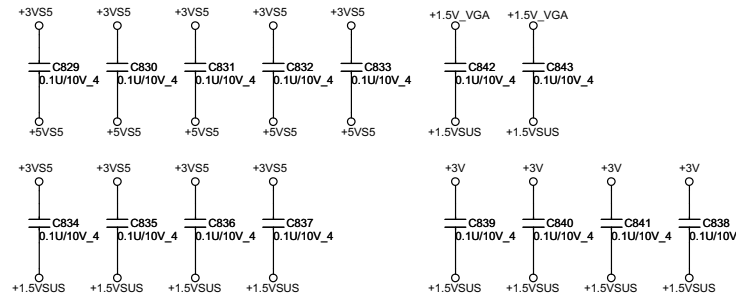
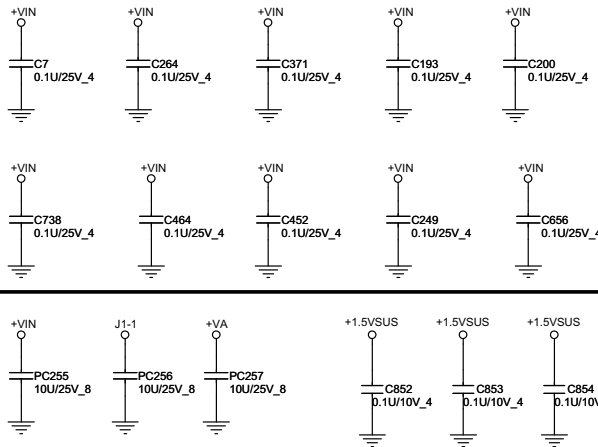
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size Custom	Document Number G-SENSOR/USB3/USB2/Charge	Rev 2A
Date: Wednesday, March 07, 2012 Sheet 26 of 42		



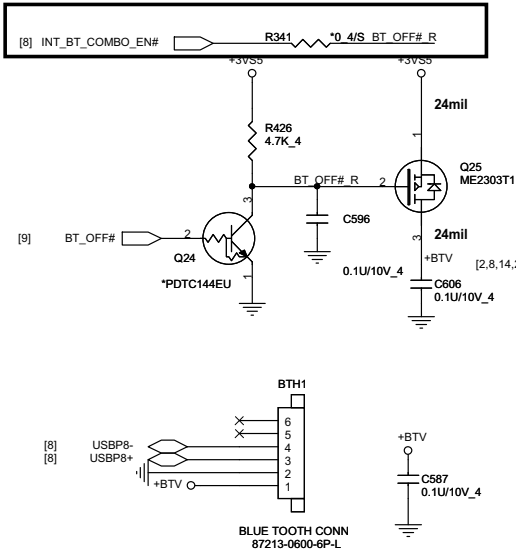
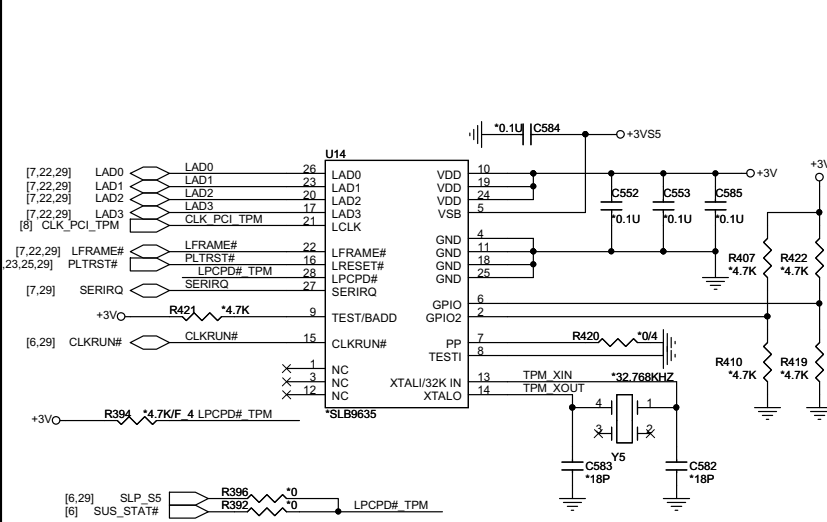
EMI CAP

DV2....Add stitch cap between power plane for EMI Request.



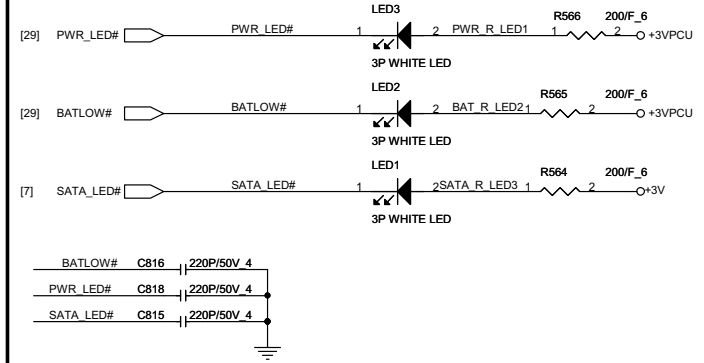
DV....Add CAP for EMI Request.

BLUETOOTH

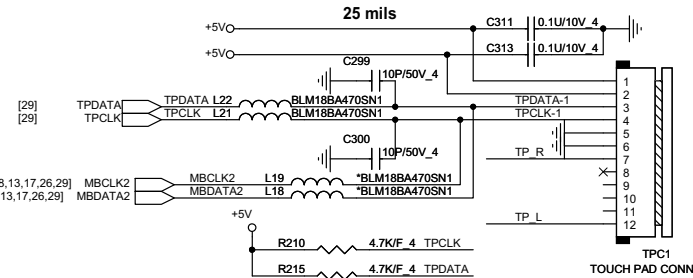
**TPM (1.2)**

LED

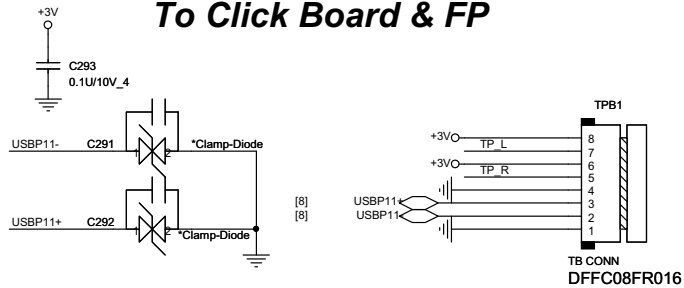
10 mils (250mA)



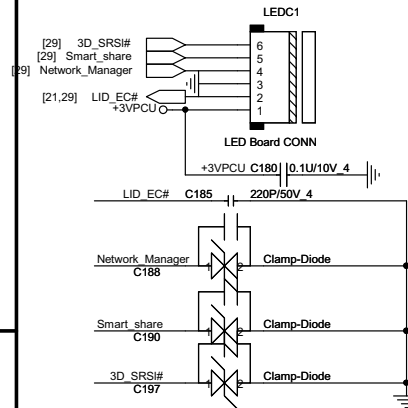
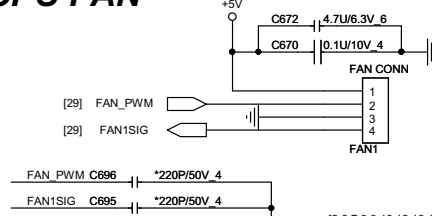
TOUCH PAD CONNECTOR To Touch Pad



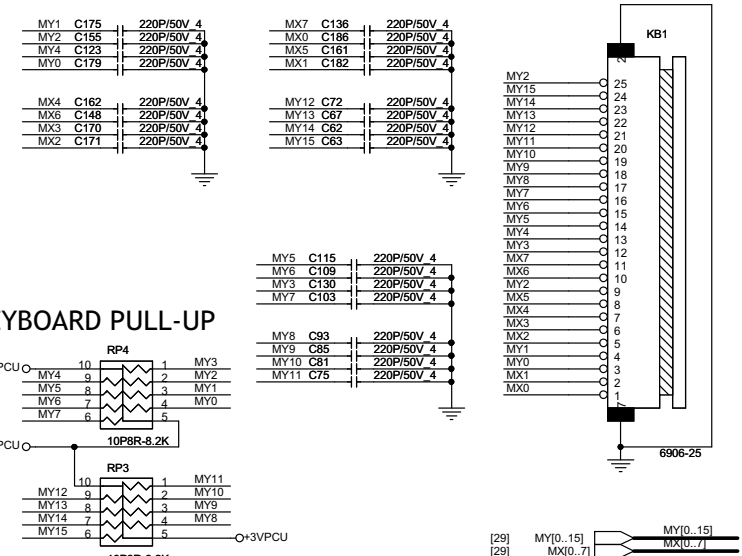
TP Button CONNECTOR
To Click Board & FP



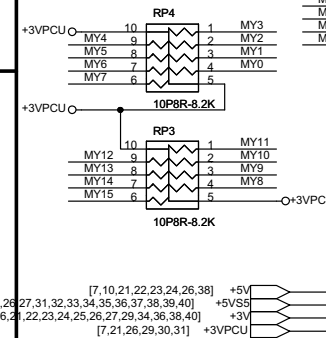
To LID Function Board

**CPU FAN**

KEYBOARD Con.



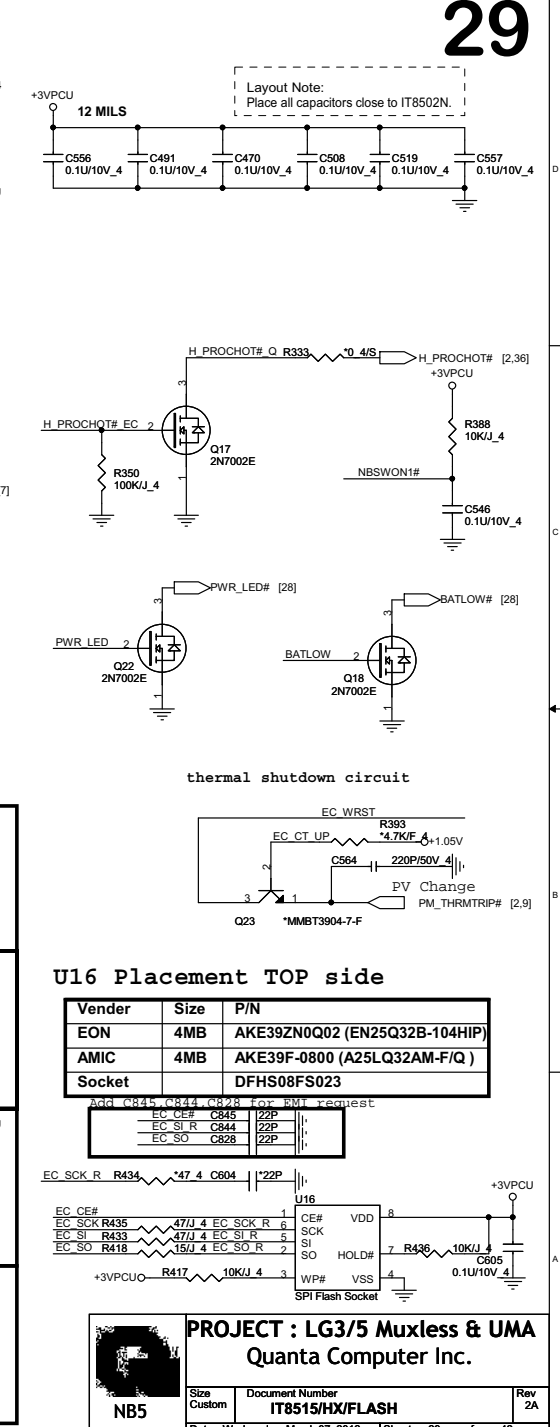
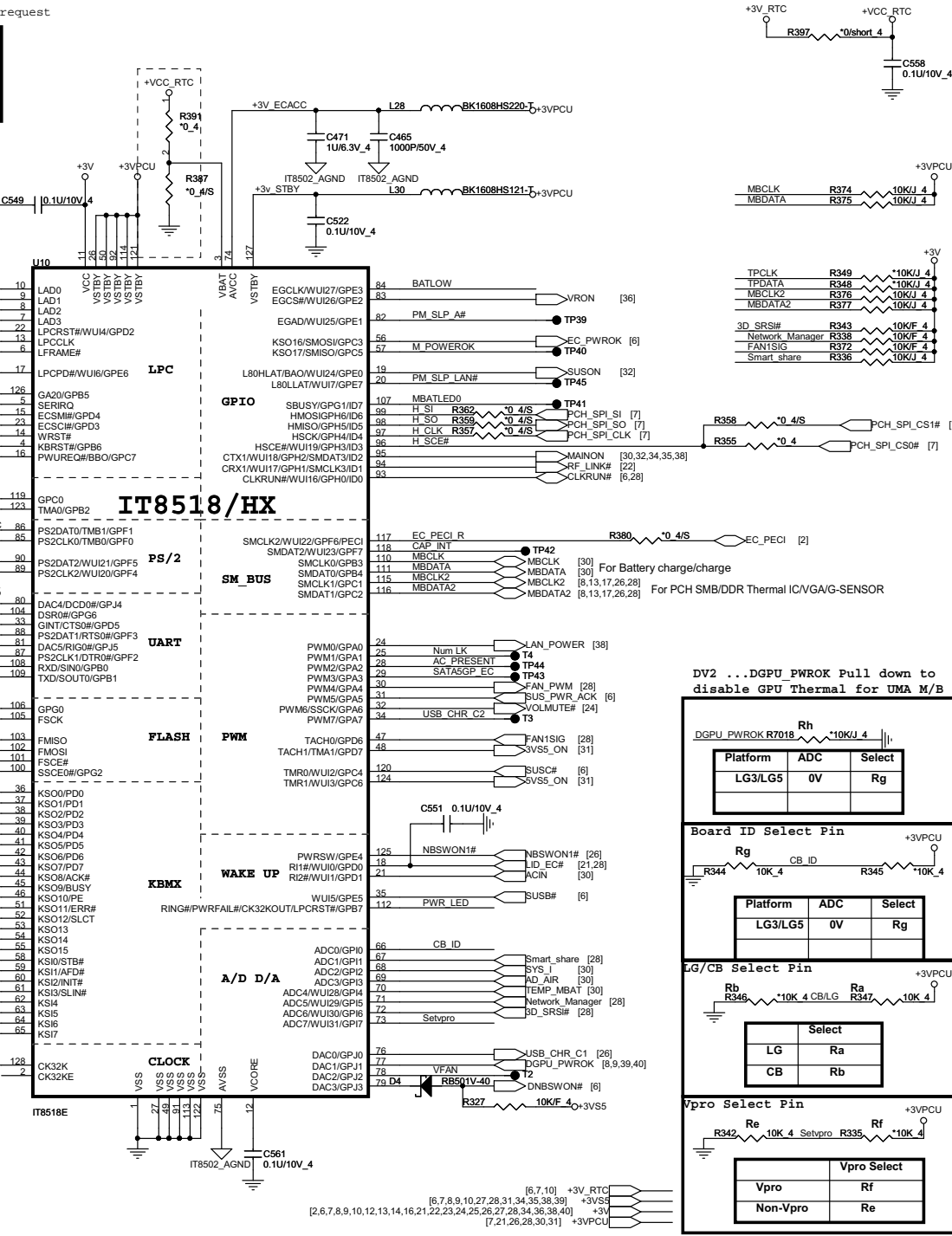
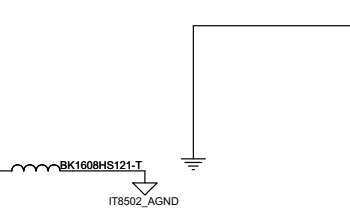
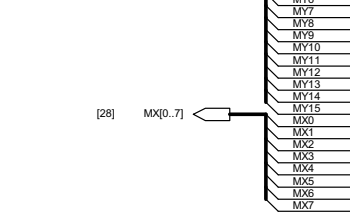
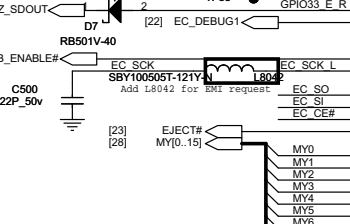
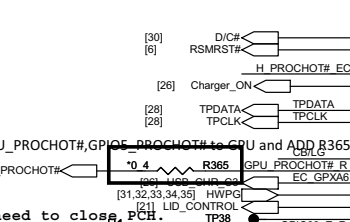
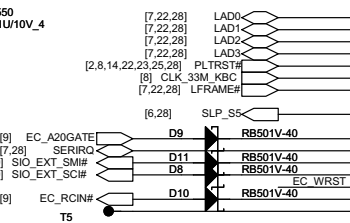
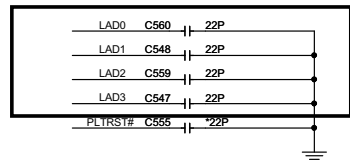
KEYBOARD PULL-UP

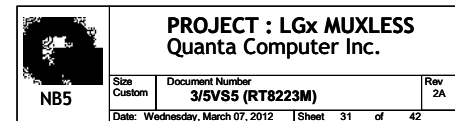


PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

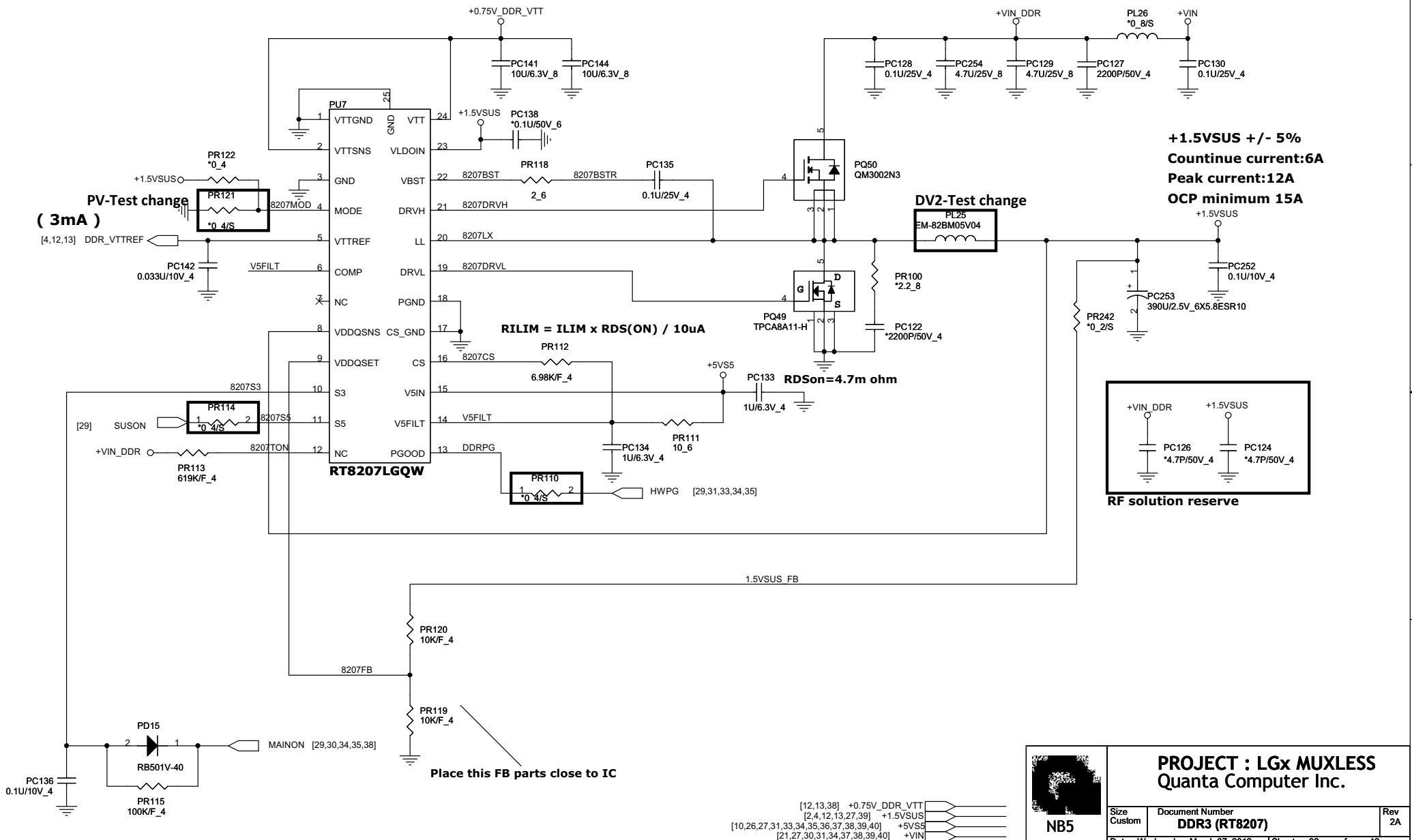
Size Custom	Document Number BT/FR/LED/TP/TPM	Rev 2A
----------------	-------------------------------------	-----------

DV2...Stuff C560,C548,C559,C547 for EMI request

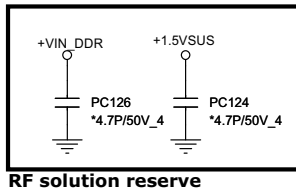




(VTT/2A)



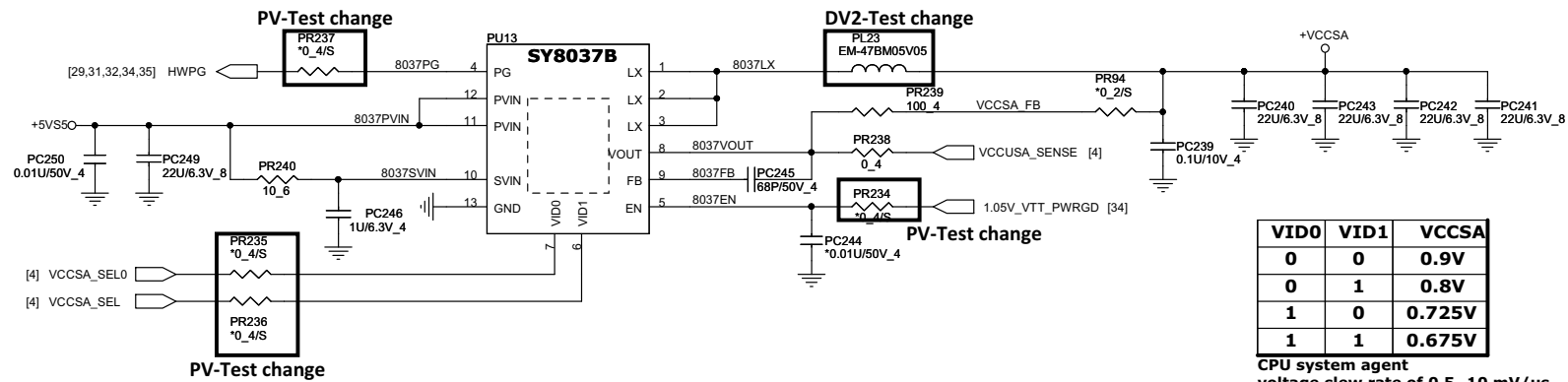
+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A



Place this FB parts close to IC

PROJECT : LGx MUXLESS
Quanta Computer Inc.

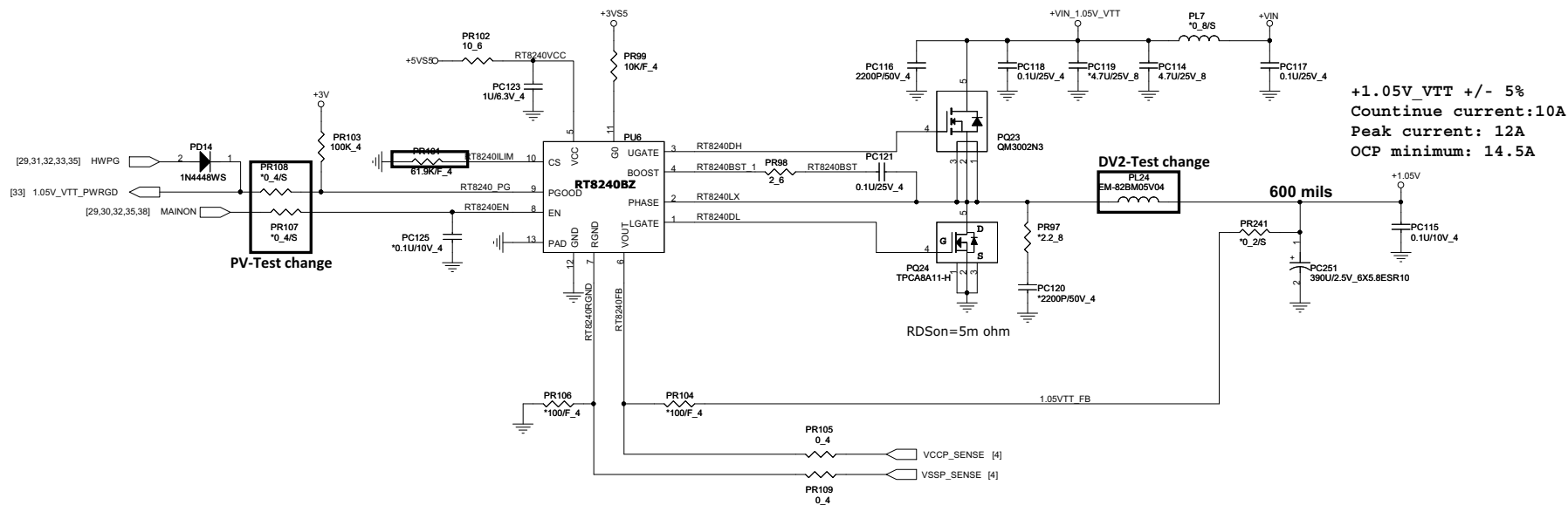
+VCCSA Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7A

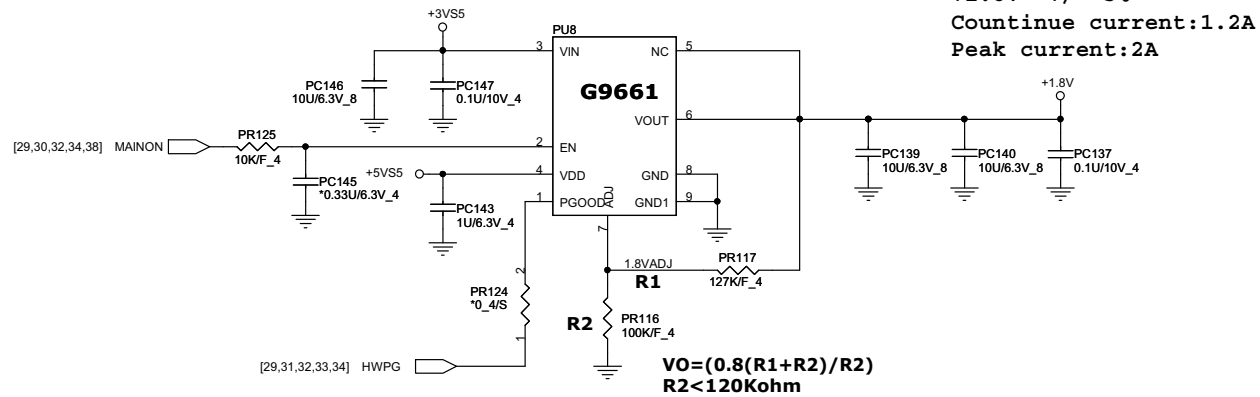


NB5

**PROJECT : LGx MUXLESS
 Quanta Computer Inc.**

Size B	Document Number VCCSA (RT8241A)	Rev 2A
Date: Wednesday, March 07, 2012 Sheet 33 of 42		

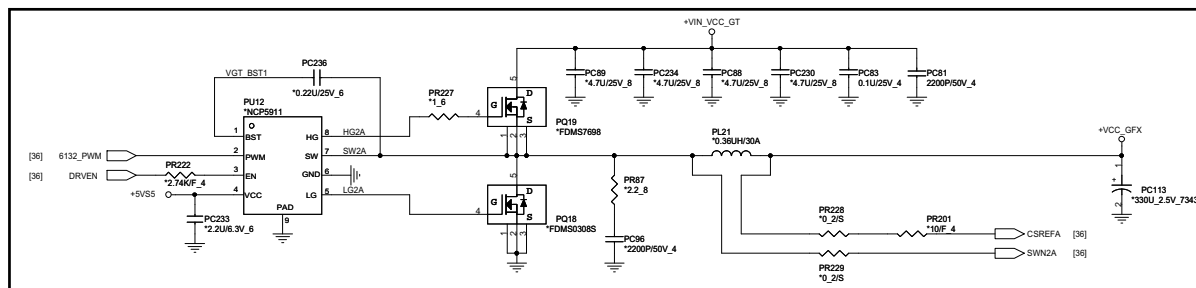
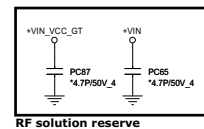
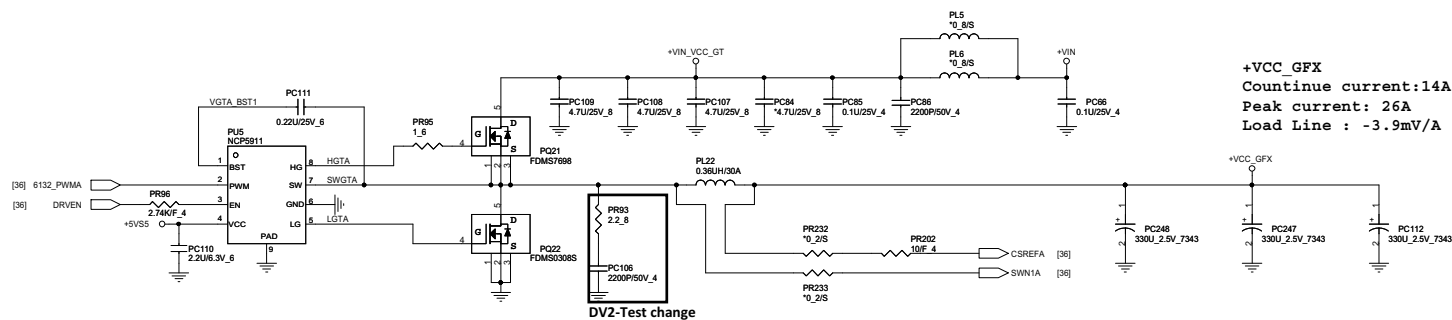
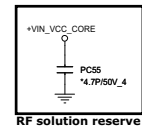
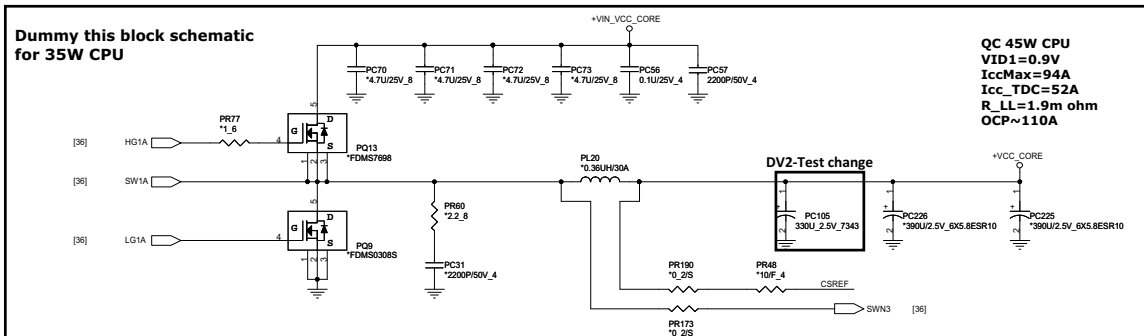
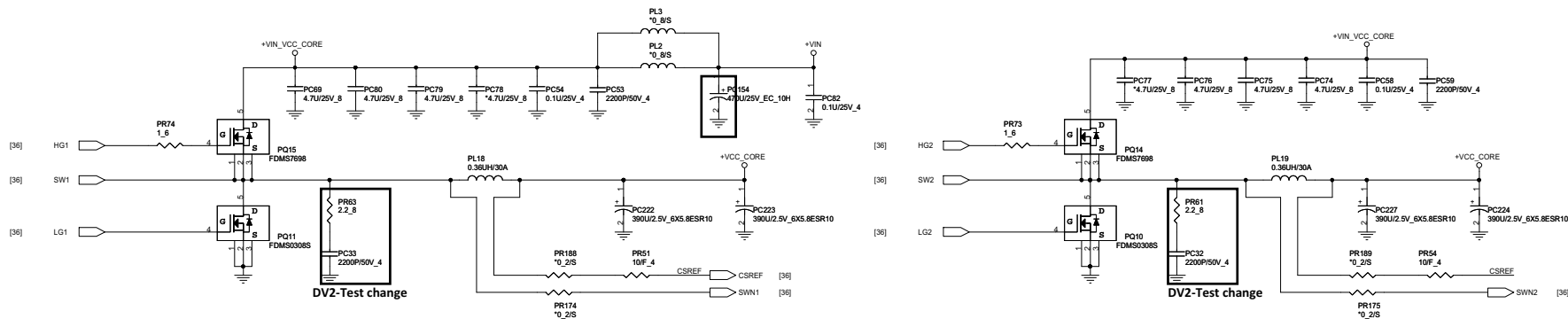




PROJECT : LGx MUXLESS
Quanta Computer Inc.

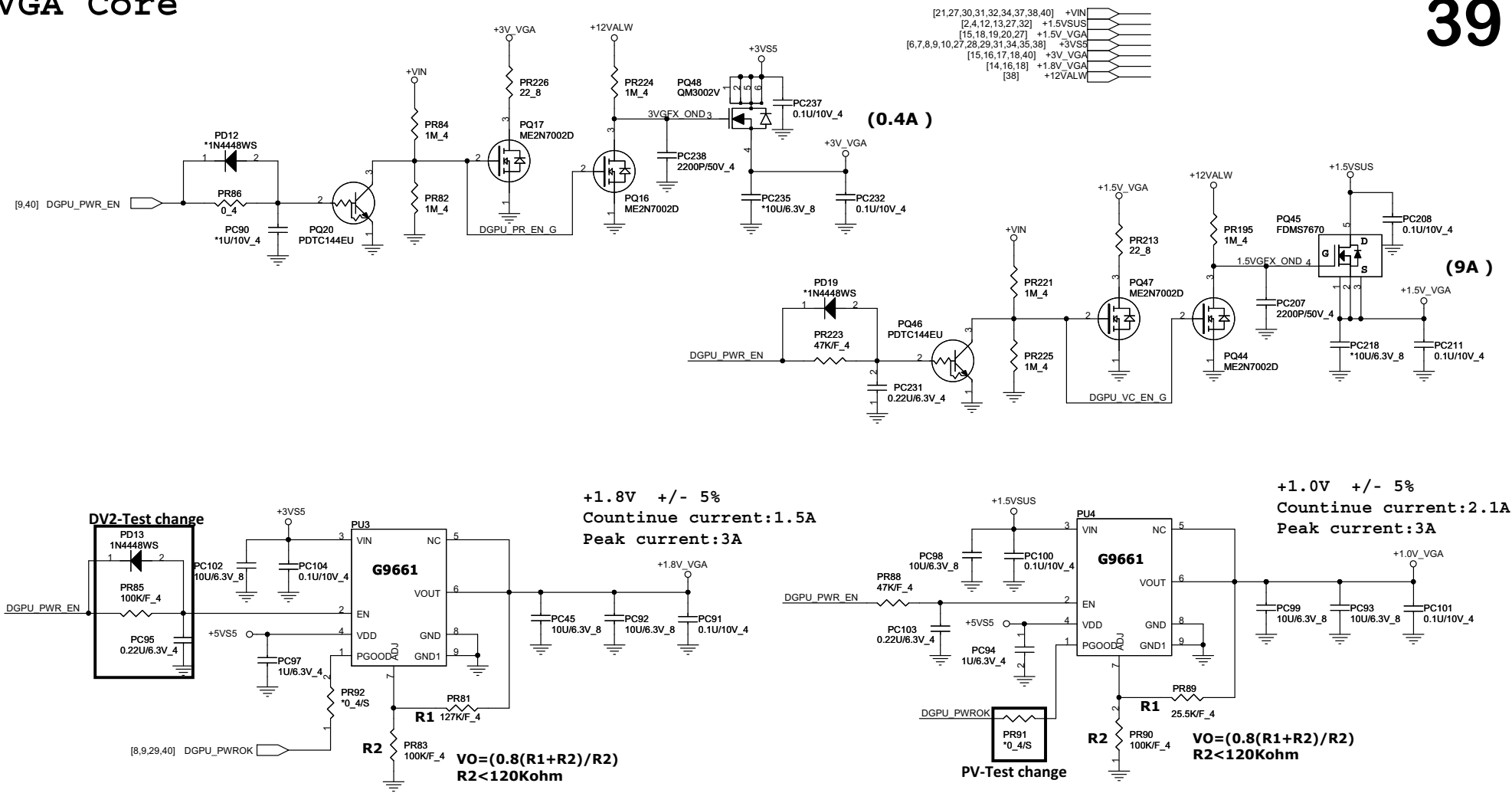
Size B	Document Number +1.8V (G9661)	Rev 2A
Date: Wednesday, March 07, 2012	Sheet 35 of 42	





PROJECT : LGx MUXLESS
Quanta Computer Inc.

VGA Core



PROJECT : LGx MUXLESS
Quanta Computer Inc.

